INTEGRATED LOW-POWER INTERFACES FOR IMPEDIMETRIC CHEMICAL SENSORS

A Dissertation
Presented to
The Academic Faculty

By

Jin-Jyh Su

In Partial Fulfillment
Of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology

December 2014

INTEGRATED LOW-POWER INTERFACES FOR IMPEDIMETRIC CHEMICAL SENSORS

Approved by:

Dr. Oliver Brand, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Hua Wang
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Jennifer O. Hasler
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Eric Vogel
School of Materials Science and Engineering
Georgia Institute of Technology

Dr. Albert B. Frazier
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: November 3, 2014

To my great family and my love Yu-Heng for their support and patience.

ACKNOWLEDGMENTS

First, I would like to sincerely express my deep appreciation to my thesis advisor, Dr. Oliver Brand. During my PhD study, I really feel lucky to have an advisor who always keeps supporting his student and providing excellent guidance the first thing in his mind. Especially, he frequently interacts and works together with his students in the lab. He gives his students a great amount of freedom in their research and always is friendly to everyone. Furthermore, I would like to thank him for his constructive opinions and encouragement not only to my research but also my personal life.

I would like to thank my dissertation committee members Dr. Jennifer O. Hasler, Dr. Albert B. Frazier, Dr. Hua Wang, and Dr. Eric Vogel for their interest in my work and their constructive advice. I would like to specially thank Dr. Hua Wang and his student Song Hu for helping me with chip measurements.

I owe a lot of thanks to Dr. Kemal S. Demirci at Texas Instrument Inc. Without his technical supports and access to Texas Instrument's processes, I could have not done my PhD research. I'd like to thank David Webb, Richard White, and T. R. Subramanian for their support with the IC design software, Bob House for his help with PCB fabrication, and Dr. Pamela T. Bhatti, her student Hakan Toreyin, and James Steinberg for supporting measurement equipments. Also, I'd like to thank my previous advisor, Dr. G. A. Rincon-Mora, for guiding me into the world of analog circuit design in an intuitive way.

I am grateful to past and present members of our research group for their help, useful discussions and friendship. Many thanks to my colleagues Dr. Luke A. Beardslee, Dr. Stuart Truax, Chris Carron, Spyros Pavlidis, Jonathan Lehmann, Karl Peterson, Pat-

rick Getz, Hommood Alrowais, and Choongsoon Kim. Especially, I would like to thank Dr. Luke A. Beardslee and Spyros Pavlidis for fabricating chemical the sensors tested in this thesis. And, for all of my friends in Atlanta, thank you for making this city a great place to live and giving me unforgettable memories.

I sincerely appreciate my parents for their patience and continuous support. I would like to express my special thanks to my in-laws for their trust, understanding, and their help in taking care of our son, Ellison. Also, I would like to thank Ellison for bringing happiness to our family and encouraging me to complete my PhD work. Finally, I would like to express my deepest gratitude to my wife Yu-Heng for her endless love, patience, encouragement, and, especially, her effort of taking care of Ellison.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

A/D	Analog-to-Digital
AC	Alternating Current
ADC	Analog-to-Digital Converter
ALD	Atomic Layer Deposition
ASIC	Application-Specific Integrated Circuit
ASM	Algorithmic State Machine
BG-switch	Body-Guarded Analog Switch
BGR	Bandgap Reference
BTBT	Band-to-Band Tunneling
CCFET	Capacitively-Controlled (or Coupled) Field-Effect Transistor
CCII	Second Generation Current Conveyor
CCO	Capacitance-Controlled Oscillator
CDS	Correlated Double Sampling
ChemFET	Chemical Field-Effect Transistors
CMOS	Complementary Metal-Oxide-Semiconductor
CNT	Carbon Nanotube
CP	Conducting Polymer
DAC	Digital-to-Analog Converter
DC	Direct Current
DDS	Direct Digital Synthesizer
DEMOS	Drain-Extended MOSFET

DIBL	Drain Induced Barrier Lowering
DR	Dynamic Range
DSM	Delta-Sigma Modulator
DSP	Digital Signal Processing
DUT	Device under Test
EDT	Edge Direct Tunneling
EMI	Electromagnetic Interference
FFT	Fast Fourier Transform
FID	Flame Ionization Detector
FSM	Finite State Machine
GC/MS	Gas Chromatography/Mass Spectrometry
IC	Integrated Circuit
IGZO	Indium-Gallium-Zinc-Oxide
INL	Integral Non-Linearity
ISFET	Ion-Sensitive Field-Effect Transistor
LDCC	Leaded Chip Carrier
LOD	Limit of Detection
LPF	Low-Pass Filter
LSB	Least Significant Bit
MCU	Microcontroller Unit
MFC	Mass Flow Controller
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MOx	Metal-Oxide

MS	Mass Spectrometer
OP	Operating Point
OPA	Operation Amplifier
PCB	Printed Circuit Board
PECH	Polyepichlorohydrin
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PEDOT:PSS	Poly(3,4-ethylenedioxythiophene)-Poly(styrenesulfonate)
PLL	Phase Lock Loop
PNOISE	Periodic Noise
PPB	Part Per Billion
PPM	Part Per Million
PSD	Power Spectrum Density
RCO	Resistance-Controlled Oscillator
REFET	Reference ISFET
RMS	Root-Mean-Square
S/H	Sample-and-Hold
SAR	Successive approximation
SC	Switched-Capacitor
SNDR	Signal-to-Noise Dynamic Range
SNR	Signal-to-Noise Ratio
SoC	System-on-Chip
TCD	Thermal Conductivity Detector
TDC	Time-to-Digital Converter

TFT	Thin-Film Transistor
TG	Transmission Gate
TRAN	Transient
VOC	Volatile Organic Compound
WSS	Wide-Sense Stationary
ZPC	Impedance-to-Pulsewidth Converter

SUMMARY

This thesis presents two interface circuits for impedimetric chemical sensors: one for passive chemical sensors and the other for ChemFETs. Both interfaces were fabricated in 0.35μm BiCMOS technology and provide the same output data rate of 1Hz.

The interface for passive impedimetric sensors is reconfigurable for performing either resistance or capacitance measurements and provides a fully digital output with less than 81.8μW power consumption at V_{DD} = 2.5V. The interface features a 176dB resistance dynamic range (31.6Ω-200MΩ, <±0.8% nonlinearity, and >40dB SNR) realized with only two sub-ranges to minimize calibration efforts and a 102dB capacitance dynamic range (0.8-1000pF, <±0.2% nonlinearity, and >40dB SNR).

The ChemFET interface is a highly versatile system that can generate a wide range of bias voltages (V_G up to 9.74V and V_D up to 16.3V depending on the measurement modes) and perform either constant voltage or constant current mode measurement. At maximum rated output (V_G = 9.74V, V_D = 16.3V, and I_{DS} = 15μA), the interface consumes only 2.02μW at V_{DD} = 3.3V and provides analog readout noise levels of 0.0476μA_{RMS} at 10μA and 0.503mV_{RMS} for I_{DS} and V_T, respectively.

Besides attempting versatile system architectures, detailed noise and efficiency analysis were performed for the passive sensor interface and the ChemFET interface, respectively. The noise analysis suggests that different types of noise (correlated or uncorrelated) dominate the noise performance in different measurement ranges and, thus, noise suppression techniques, such as chopper stabilization, correlated double sampling (CDS), and oversampling/averaging, are applied to adequate parts of the interface system. The

efficiency analysis of the boost capacitor charger in the ChemFET interface concludes that applying a moderate pulsewidth (200-300ns) to drive the boost converter yields the best efficiencies for charging a capacitor.

Compared to interfaces described in the literature, the proposed interface for passive sensors achieves better versatility and wide dynamic range with less number of sub-ranges and power consumption. The proposed interface for ChemFETs achieves wider voltage supply range at very low power level.

In-house fabricated chemical sensors, including passive chemical sensors and ChemFETs, were interfaced with the developed circuits and gas-phase chemical measurements with the systems were demonstrated. The novel passive chemical sensor tested in this thesis employs a multi-functional design, which can be configured into either a chemoresistor or a chemocapacitor; the tested ChemFET employs a bottom-gate TFT structure to allow the semiconducting film to interact with the analytes.

CHAPTER 1

INTRODUCTION

Chemical sensors are a group of sensors transferring qualitative and/or quantitative information of chemical substances into processible signals. Frequently, chemical sensors consist of a *sensitive layer* made up of one or multiple sensing materials whose physical and/or chemical properties are changed upon interacting with *analytes* of interest, and a *transducer* to convert these property changes into a desired signal domain, e.g., an electrical signal. The sensitive layers are preferably composed of materials exhibiting a high affinity to the target analytes. When sensitive layers are part of a chemical sensor, the role of the transducer is to perform a signal conversion of changes in the sensing material properties such as mass, impedance, enthalpy, work function, or Seebeck coefficient. However, certain types of chemical sensors (e.g., optical, or spectrometers) are able to directly detect fundamental physical or chemical properties of the analytes without the aid of sensitive layers. Regardless of the used sensing mechanisms, the sensor output signal generally further processed so that the user can easily interpret it. Hence, chemical sensors are usually not used alone, but they serve as the front-end device of a chemical sensing system.

1.1 Chemical Sensing Systems and Impedimetric Chemical Sensors

Figure 1.1 shows a typical *chemical sensing system* consisting of a chemical sensor and a *signal processor*. Since chemical sensors are analog devices, the signal processor usually contains electronic circuits that perform some of the following analog signal

processing and/or sensor control functions: signal amplification, filtering, analog-to-digital (A/D) conversion, temperature control, sensor excitation, and sensor modulation. Signal processors based on this narrow definition are often called sensor *interfaces*; however, the broad definition of a chemical sensing system also incorporates all data analysis and system calibration blocks that perform advanced functions in the digital domain. Depending on the sensing mechanisms and complexity of the applications, the signal processor could be a laptop or desktop computer, which ultimately dominates the size of the whole sensing system.

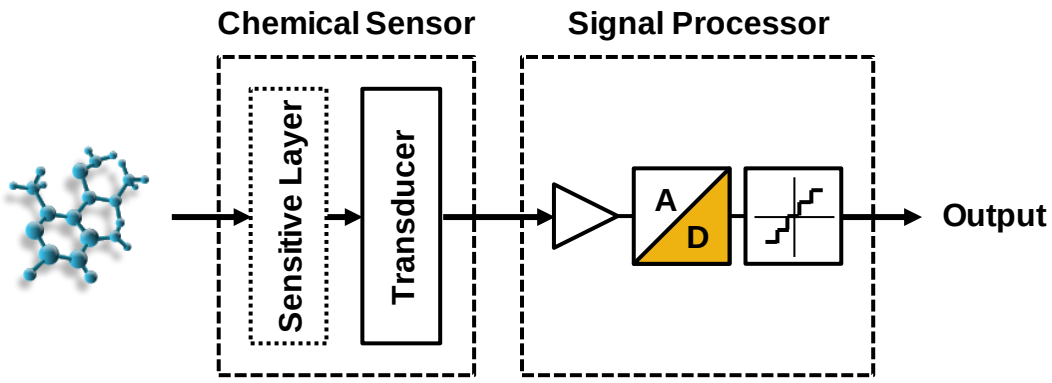


Figure 1.1: General structure of a chemical sensing system.

The performance of chemical sensing systems can be assessed in terms of their *sensitivity* and *selectivity*. Together with the system *noise*, the former determines the *limit of detection* (LOD) of the chemical sensing system, while the latter implies the immunity of the system to unexpected analytes or its ability to analyze chemical mixtures. The LOD, which is usually quantitatively represented in parts per million (ppm) or parts per billion (ppb), is limited by the sensitivity and the noise of the sensor itself and the additional noise coming from the signal processing circuits. The total system noise may be

minimized with superior signal processing techniques and sensor control algorithms. In the presence of sensitive layers, the sensor selectivity strongly depends on the properties of the sensing materials; however, the selectivity can be improved on a system level using pattern recognition algorithms [1] and proper sensor modulations [2]. Sensing systems that directly detect a fundamental (molecular) property of analyte (e.g., its absorption spectrum or its molecular mass) typically exhibit excellent selectivity.

One of the most widely employed chemical sensing systems are gas chromatography/mass spectrometry (GC/MS) systems [3] shown in Figure 1.2(a). A GC/MS system is comprised of a gas separation stage followed by a sensitive chemical sensor, in this case a mass spectrometer (MS); however, flame ionization detector (FID) or thermal conductivity detector (TCD) can also be used in conjunction with the GC unit. GC/MS systems achieve high selectivity and sensitivity (with LODs in the ppb range or even below with proper pre-concentration stages) and are often considered the gold standard of chemical analysis. In the case of GC/MS systems, the signal processor is a complex computing system that controls the complex measurement sequence and performs the multi-functional data analysis. Such bench-top instruments exhibit excellent performance over a wide range of analytes and analyte mixtures, but they are bulky, expensive, (often costing more than $30,000), and require trained personnel for operation. As a result, GC/MS systems are often found in analytical laboratories rather than in the field. For many applications, such as indoor toxic gas detection, water quality monitoring, or a sobriety test, system portability is more important than the ultimate sensitivity and selectivity, and thus, hand-held sensing systems [4], as the one shown in Figure 1.2(b), provide a better solution. Hand-held chemical sensing systems often exhibit more limited selectivi-

ty (and sensitivity), and are typically able to detect a limited number of target analytes, rather than performing a complex chemical analysis. Instead of using complex GS/MS systems, hand-held sensing systems usually employ small-size and low-cost optical sensors (e.g., photo ionization detectors, infrared sensor) or sensitive-layer-enabled electrochemical sensors [4, 5]. In this case, the signal processor often is a mixed-signal microcontroller that performs only essential signal conditioning and data analysis. Depending on the applications and system capabilities, the cost of hand-held chemical sensing systems is in the range of hundreds to several thousand dollars. It should be noted, that recent research efforts are also targeting the development of GC-based sensing systems in a hand-held format [6]. So far, the GC/MS systems and the hand-held gas detectors being discussed are limited to scientific instruments for professional purposes, whereas simple chemical sensing systems are widely found in households. The most well-known device is the fire detectors [7], shown in Figure 1.2(c), which more and more often are multi-sensor systems composed of smoke sensors, hazardous gas sensors, and light sensors. Unlike professional instruments which are required to display reliable and accurate analyte concentrations, the gas sensors employed in fire detectors are relatively low cost electrochemical sensors and the interface can be as simple as an electronic arbiter that determines the alarm triggering level. Thus, they are affordable in residential applications, costing around $100 or less.

(a)  (b)  (c) 

Figure 1.2: (a) Agilent 7000A GC/MS system [3] (b) RKI Eagle 2 gas detector [4] (c) Nest smoke and carbon monoxide detector [7].

In recent years, chemical sensing systems have attracted substantial interest in military, automobile, medical, and personal electronic industries. However, the oversized and pricy sensing systems based on conventional fabrication and printed circuit board (PCB) technologies no longer satisfy many of today's application requirements. With the advance of microfabrication technologies, ubiquitous chemical sensing systems in areas such as implantable bio-medical devices, in-situ environment monitoring networks, and next generation portable electronics, are becoming feasible. Thereby, microfabrication and system-on-chip (SoC) technologies provide promising approaches to implement the whole sensing system on one or few silicon chips. These technologies benefit from low manufacturing and assembling costs as well as ease of mass production. One of the first demonstrations of a highly integrated chemical sensing platform dates back to the early 2000's (Figure 1.3), with multiple microfabricated chemical sensors and associated inter-face and communication circuits built on a single chip [8]. It is not far reaching that, in the near future, advanced features such as wireless transceivers will be co-integrated with on-chip chemical sensing systems to provide real-time communication and inter-sensor

data exchange, pushing chemical sensing systems into a whole new era.

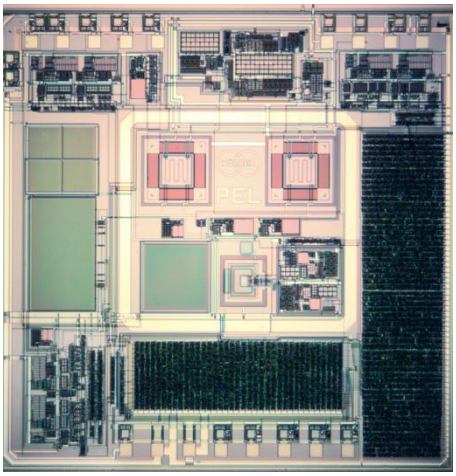


Figure 1.3: Chemical sensing system based on SoC technology [8].

Microfabricated chemical sensors, or simply known as *chemical microsensors*, are often classified by their underlying sensing principle as mass-sensitive, thermal, optical, and electrochemical sensors [9]. Among the various sensing mechanisms, the sub-group of electrochemical sensors providing impedance responses, e.g., *chemoresistors*, *chemocapacitors*, and chemical field-effect transistors (*ChemFET*), are of particular interest to this work. (In the following chapters, these three types of sensors are called *impedimetric sensors*, while chemoresistors and chemocapacitors together are also called *passive impedimetric sensors* as they are essentially passive electronic components.) Key advantages of these impedimetric microsensors are that (1) they typically have a simple device structure comprising (interdigitated) metal electrodes or a field-effect transistor and that (2) impedance changes can be easily processed with electronic circuits. The simple device structure enables the fabrication of impedimetric chemical microsensors with mainstream complementary metal-oxide-semiconductor (CMOS) microfabrication tech-

nologies. In many cases, incorporating impedimetric chemical sensor fabrication into a standard CMOS process flow requires only slight (or even no) modifications of CMOS technology or little additional back-end processes. Furthermore, different impedimetric *sensor arrays* have been realized with microfabrication technologies [10-12] (see Figure 1.4), and thus the system selectivity can be improved with signal post processing of multi-dimensional data.

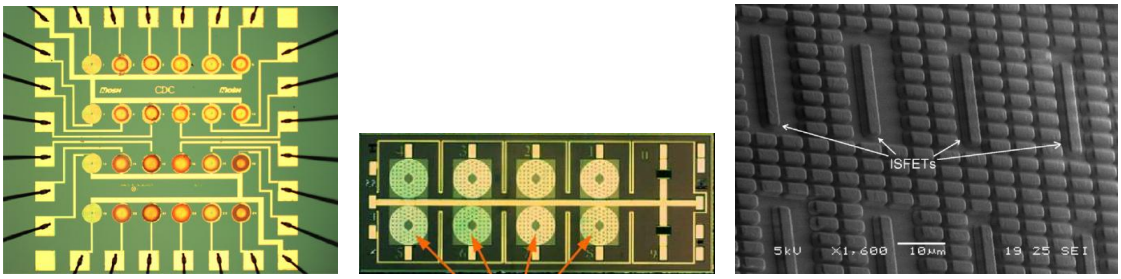


Figure 1.4: Impedimetric chemical microsensor arrays of, from left to right, chemoresistor [10], chemocapacitor [11], and ChemFET [12].

The continuous scaling of chemical sensing systems using microfabrication technologies and in particular CMOS technologies has, e.g., enabled the integration of humidity sensors in recent Samsung Galaxy phones [13] and will open new applications in the biomedical and environmental monitoring fields. One of the main challenges in these fields is the power consumption, as these systems are often battery-operated and are required to survive for years. Undoubtedly, reducing power consumption becomes a priority in sensor interface design. Although the performance (e.g., power consumption, accuracy, dynamic range) of sensor interfaces could be optimized by making a dedicated design for a specific sensor, the fact that different impedimetric chemical microsensors cover a wide range of impedances, would require an interface circuit redesign for each

sensor. Consequently, this work focuses on a versatile system that adapts to both resistance and reactance over a wide range of values.

Even though CMOS interface circuits with power consumption in the micro-Watt range have been realized for different applications [14], operating at low power as well as maintaining sufficient resolution and linearity over a wide range is a great challenge. In this research, the ultimate goal is to implement battery-powered chemical microsensor interfaces that achieve aforementioned versatility based on commercial CMOS technology. Besides power consumption and impedance characteristics, other issues such as long-term stability will be also discussed and considered in the system level design. Because of the significant differences between passive impedimetric sensors and ChemFETs, two separated systems were implemented for each category of chemical microsensors. The performances of both interfaces are initially characterized with conventional board-mounted electronic devices (i.e., commercial chip resistors and capacitors). Afterward, gas phase chemical measurements with volatile organic compounds (VOCs) were carried out in a customized gas measurement setup by interfacing both in-house fabricated microsensors and commercial chemical sensors to the developed interface circuits.

1.2 Outline of Thesis

The objective of this thesis is to develop versatile application-specific integrated circuits (ASICs) for impedimetric chemical microsensors using commercial CMOS technology. The thesis follows the logic of understanding characteristics of chemical microsensors, defining interface circuit specifications, surveying state-of-the-art interface circuitry, introducing in-house fabricated chemical microsensors, designing and analyzing

proposed interfaces, and performing practical chemical measurements.

Following this introduction, the first half of Chapter 2 discusses various types of chemoresistor, chemocapacitor, and ChemFETs. Sensor specifications are gathered and categorized to define a set of specifications for both interfaces, the passive impedimetric chemical sensors and ChemFETs. The second half of Chapter 2 devotes to a thorough literature survey of interfacing techniques for chemical sensors based on integrated circuit technology.

Chapter 3 gives a brief introduction of an in-house fabricated multi-function passive impedimetric sensor and an emerging thin-film transistor (TFT) sensor. These sensors are later interfaced with the proposed circuits to perform gas measurements.

Chapter 4 introduces the first proposed interface for passive impedimetric chemical sensors. The chapter first presents the core idea of the proposed system. Next, the advantages of the proposed system are compared with conclusions drawn from the literature survey to explain the way that final approach is chosen. Afterwards, each block is discussed and analyzed in detail, supported by simulation and measurement results, to determine the suitable techniques for improving noise performance. Finally, the full system is characterized over a wide range of resistors and capacitors and the important system metrics, such as linearity, noise level, and signal-to-noise ratio (SNR) are established.

Chapter 5 begins with a short discussion of system requirements and possible solutions. Then, an overview of proposed interface is presented. The next two sub-chapters are dedicated to major contributions and innovations of the proposed system: the analysis of (1) a pulse-mode capacitor charger and (2) a low-leakage body-guarded switch (BG-switch). The functionality of the system is characterized using a commercial met-

al-oxide-semiconductor field-effect transistor (MOSFET).

Chapter 6 describes a customized chemical measurement setup and the measurement results of interfaced sensors. The measurements were carried out with in-house fabricated chemoresistors, chemocapacitors, and ChemFETs. Additionally, we performed gas measurement with a purchased chemoresistor for sensing alcohol to serve as reference measurement results.

Chapter 7 concludes the research and suggests several future directions.

CHAPTER 2

IMPEDIMETRIC CHEMICAL SENSORS AND INTERFACE CIRCUITRY

The literature research chapter is divided into two major parts: impedimetric chemical sensors and sensor interfacing techniques. Although this thesis focuses on the circuit side, understanding basic sensing mechanisms and sensor characteristics is essential for circuit engineers in order to make a practical and high-performance design. In other words, without a fundamental knowledge of impedimetric chemical sensors, engineers cannot generate proper circuit specifications and implement optimum sensor control. Consequently, the literature survey of interfacing techniques should come after summarizing sensor characteristics. The goal of realizing a versatile sensing system cannot be accomplished by employing any one of the existing techniques. Rather than focusing on a single circuit parameter, the purpose of the literature research on interfacing techniques is to summarize their topological advantages and individual circuit tricks, which ultimately helps determine the system design approach and improves circuit performance.

2.1 Impedimetric Chemical Sensors

From circuit engineer's point of view, impedimetric chemical sensors can be categorized into three groups: chemoresistors, chemocapacitors, and ChemFETs. This classification is based on the differences in electrical properties and interfacing approaches, e.g., probing the response to alternating currents (AC) or direct currents (DC) or the

number of device terminals used. Although each group contains thousands of particular sensor implementations, the purpose of the literature survey is to establish general sensor specifications and not to provide an exhaustive survey of impedimetric sensors. Thus, a brief explanation of the sensing mechanisms and a summary of their electrical properties are the focus of this sub-section.

2.1.1 Chemoresistors

The most well-known group of chemoresistors is metal-oxide (MOx) gas sensors, which are often employed in smoke detectors for carbon monoxide sensing. The first demonstration of MOx sensors can be traced back to 1962 when Tetsuro Siyama and Naoyoshi Taguchi proposed gas sensors employing ZnO semiconductive films as sensitive layer [15, 16]. Because of their appealing characteristics, such as low cost, small size, fast response time, and reliability, MOx sensors have been widely studied and commercially available for several decades. MOx sensors are used for detecting reducing gases based on a chemical redox reaction taking place at the surface of the MOx film, which results in a decrease in film resistivity [17]. This mechanism is depicted in Figure 2.1. The MOx films are usually intrinsically n-type poly crystalline semiconductors that conduct electrical current by tunneling electrons through the boundaries of crystallitic grains. In the atmosphere at elevated temperature (above 420K), oxygen and water vapor is ionized, resulting in O^- or O^{2-} adsorbed on the surface of the MOx films. Via the field effect, the adsorbed oxygen ions induce a thin depletion region in nanometer range around the crystallites, which causes an increase in the tunneling barriers between grains (0.5-1.0eV) and, hence, increases film resistivity. Normally, the baseline resistance (i.e., resistance

without the presence of targeting analytes) of MOx sensors ranges from hundreds of kΩ to hundreds of MΩ, depending on the film material and film structure. In the presence of reducing gases, the pre-adsorbed oxygen ions react with the reducing gas molecules, resulting in a decrease of the depletion region width and, hence, film resistivity.

MOx chemical sensors usually show excellent sensitivity because the film conductivity increases exponentially in response to the decrease in tunneling barriers, causing large changes in film resistance. The decrease of the sensor resistance when exposing to hundreds of ppm of target analytes is often more than an order of magnitude from the baseline values, which is allows detecting low (often sub-ppm) analyte concentrations [18]; however, the large resistance change can easily saturate an interface circuit whose dynamic range is not sufficient. Furthermore, MOx sensors typically require heaters for operation at elevated temperature, consuming at least milli-Watts of power, to activate the ionization process of adsorbed oxygen. It should be noted, however, that recently reported MOx sensors employing noble metal (platinum and palladium) catalysts are able to operate at room temperature [19].

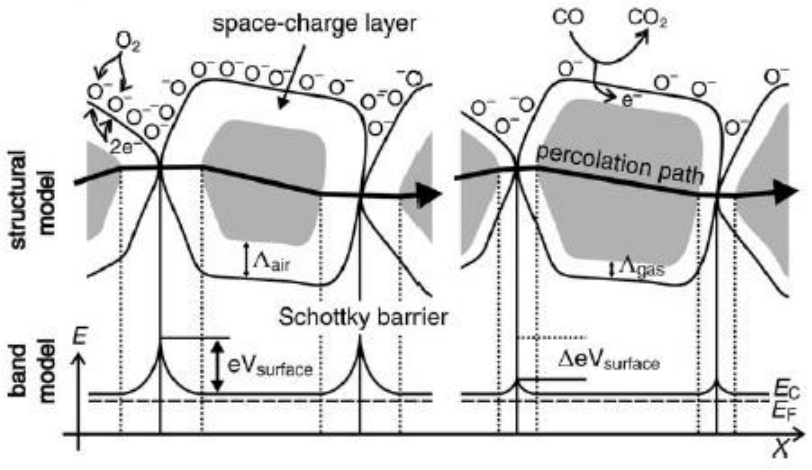
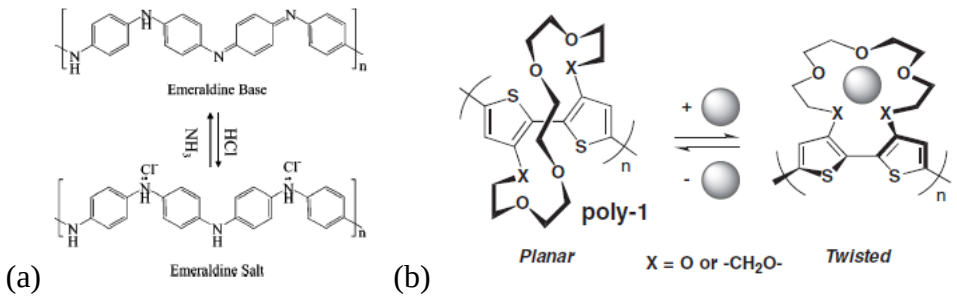


Figure 2.1: Sensing mechanism in MOx sensitive layer [17].

Another group of chemoresistors is based on conducting polymer (CP) sensing films and CP nanofibers. They have been demonstrated in various applications, such as pH sensors and gas sensors [20]. CPs are non-conductive in their original state, but can be made conductive by doping through electro-chemical oxidation (p-doping) and reduction (n-doping) along their conjugate backbones. The redox level and any associated modifications during or after the redox reaction strongly affect the electrical characteristics of CPs (i.e., semiconductive or metallic). Semiconductive CP chemoresistors have high baseline resistances and exhibit strong responses similar to MOx sensors, while metallic forms of CPs (e.g., polyaniline emeraldine salt) can exhibit baseline resistances in range of hundreds ohms and sensor responses in low percentage ranges.

The way that CP sensors interact with analytes is believed to be a complex physicochemical mechanism. Physically, the absorption of analytes causes film swelling and, thus, stress in the polymer chain structure, which leads to a change in sheet resistivity and carrier mobility; chemically, multiple theories, such as redox reactions and twist bindings shown in Figure 2.2, have attempted to explain how the doping level is modulated by analyte absorption [21, 22]; however, details of most chemical reaction mechanisms are still unclear. In contrast to MOx sensors, most CP sensors can be operated around room temperature. However, CPs suffer from poor reproducibility and strong long-term conductivity drift because of film degradation. Possible reasons for this sensor drift include irreversible chemical reactions between CPs and analytes, oxygen, or humidity [23], heating effects, and polarization effects associated with constant DC biases [24]. Degradations caused by chemical reactions remain a considerable challenge, while the thermal and polarization effects suggest interface designers to use low current AC excitations.



(a) (b)

Figure 2.2: (a) Redox reaction [21] and (b) twist binding between analyte and CP [22].

In recent years, high surface area-to-volume ratio carbon-based nanostructure materials, including carbon nanotubes (CNTs), carbon blacks, and graphene, have been enthusiastically studied as impedimetric chemical sensors [25]. Carbon nanomaterials can be either dispersed in an insulating/conducting polymer matrix or employed in raw (or modified) formats. CPs loaded with carbon nanomaterials exhibit similar electrical properties and sensing mechanisms as CP sensors mentioned in the previous paragraphs, while they show strongly enhanced sensitivity [26]. Current flow in composites of carbon nanomaterials and insulating polymer composites relies on the pathway created by the conductive carbon molecules. The polymer material serves as an absorbent material whose volume increase as a function of the amount of analytes being absorbed. Figure 2.3(a) shows how this swelling effect causes a disruption of conducting paths and, thus, a decrease in film conductivity. Some composite sensors achieve LOD in the part per trillion (ppt) range [27] and show small degradation [28] in the atmosphere because of the physical sensing mechanisms. Sensitive layers of raw or catalyst-modified carbon nanomaterials, mostly carbon nanotubes (CNTs), also exhibit ppb-level LOD [29]. Simulation results suggest that the sensing mechanism of CNTs could be surface charge density redistributions due to chemical bindings [30] (Figure 2.3(b)), which ultimately leads

to a change in CNT conductivity. Sensors employing carbon nanomaterials often show conductivity change of several decades at ppm analyte level, implying excellent LODs. Consequently, the required interface dynamic range of carbon nanomaterial sensors is similar to MOx sensors.

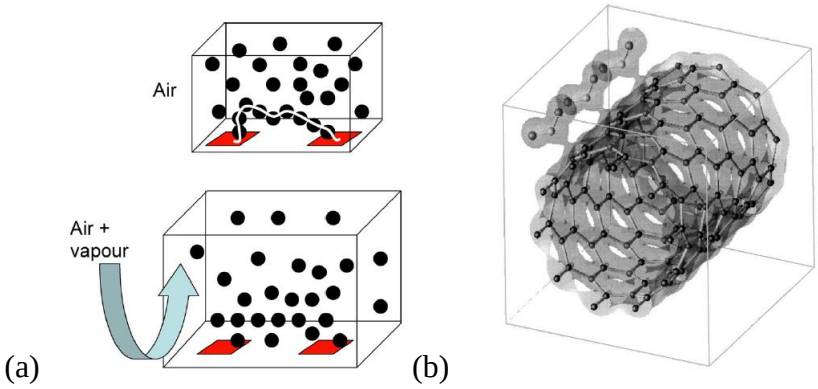


Figure 2.3: (a) Swelling effect in composites of carbon nanomaterial and insulating polymers [25] and (b) charge density plot of CNT with chemical bindings [30].

2.1.2 Chemocapacitors

Capacitive sensors exhibit multiple attractive advantages to engineers. Circuit engineers treat chemocapacitors as a charge-based device that consumes approx. nanojoules in a single readout. From a process engineer's point of view, the only difference between chemocapacitors and traditional capacitors is the dielectric material being replaced with the sensing material. Thus, chemocapacitors can be a simple parallel plate or interdigitated electrode structure, which are easy to implement with existing metal and passivation layers in commercial CMOS technologies. In terms of sensing material, chemocapacitors employ dielectric sensing films, mostly insulating polymers or porous oxide mixtures, and operate at room temperature. In general, chemocapacitors exhibit a

better long-term stability compared to CPs and MOx sensors. As the name suggests, the capacitance of a chemocapacitor changes in response to the absorption of target analyte. This sensor response can be attributed to two sensing mechanisms: (1) the change of the sensing film's dielectric permittivity and (2) the film swelling due to the analyte absorption [31]. Figure 2.4 illustrates both effects in an interdigitated chemocapacitor. Depending on electrode pitch, film thickness, and sensing material (e.g., polymer or hard oxide mixture), one mechanism may dominate the other.

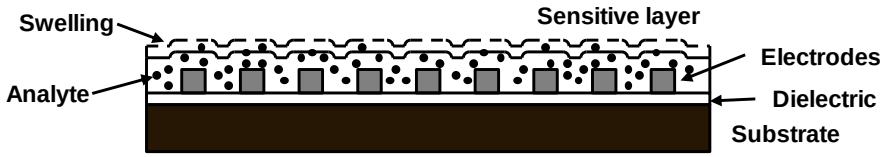


Figure 2.4: Analyte absorption and swelling effect in interdigitated chemocapacitor.

Chemocapacitors have been demonstrated for humidity, VOCs, and greenhouse gas sensing. Because of the high relative permittivity of water (~78.5), chemocapacitors are frequently considered the most promising solution for humidity sensors. Most chemocapacitors undergo chemical reaction-free sensing mechanisms and, hence, they show outstanding performances in terms of long-term drift and reproducibility; however, their major drawback is their generally low sensitivity. Microfabricated chemocapacitors normally show a capacitance changes in a few percent range upon exposure to thousands of ppm of analyte with baseline capacitances in the pico-Farad range [32], which implies that interface circuits must resolve femto-Farad capacitance changes. Some publications report that the sensitivity may be significantly improved with nanostructure sensing materials [33, 34]. In [33], 500ppm of ethanol results in a capacitance increase of 430%.

2.1.3 Chemical Field-Effect Transistor (ChemFET)

ChemFETs are electrochemical sensors that evolve from traditional MOSFET structures. They include floating-gate ion-sensitive field-effect transistors (ISFETs) and chemical sensors based on TFT technology. A structure called capacitively-controlled (or coupled) field-effect transistor (CCFET) that combines an air-gap chemocapacitor with a FET is often considered a type of ChemFET [35, 36]. In industry, ISFET pH sensors have been commercially available for at least a decade; in academia, ChemFETs have been demonstrated in various applications, including as gas detectors and biomedical sensors [35]. The gate or body terminals of ChemFETs normally serve as interface to the sensitive layers where analyte absorption/adsorption takes place, resulting in change of material properties, and thus threshold voltage (V_T). This sensing mechanism is governed by the following generalized V_T equation [37]:

$$V_T = \frac{\Phi_G - \Phi_{Sub}}{q} - \frac{Q_{ss} + Q_B - Q_{ox}}{C_{ox}} + 2\phi_F \tag{2.1}$$

where q is the electron charge, C_{ox} is the gate capacitance per unit area, ϕ_F is the Fermi level of substrate, Φ_G and Φ_{Sub} are work functions of the gate and substrate materials, respectively, and Q_{ss}, Q_B, and Q_{ox} are surface state density, depletion-layer charge, and fixed oxide charge, respectively. The sorption of analyte on the gate electrode causes a change in Φ_G, while the sorption of analyte on the body results in change in Φ_{Sub} and ϕ_F, or even the carrier mobility in the channel, which is not shown in the above equation. In the ISFET case, the gate conductor is removed and replaced by a floating reference electrode in contact with liquid, allowing the gate oxide to interact with liquid. In this case, Φ_G can be split into several terms related to liquid-solid interfaces [37]:

$$\frac{\Phi_G}{q} = E_{ref} - \Psi_0 + \chi_{sol} \tag{2.2}$$

where E_{REF} is the reference electrode potential relative to vacuum, Ψ_0 is the oxide surface potential, and χ_{sol} is a constant of the dipole potential of the solution. The binding of hydrogen ions to the gate oxide causes Ψ_0 to decrease linearly with logarithmic hydrogen ion concentration in the liquid. Conducting polymers, ceramics, metal oxides, and carbon nanomaterials are popular gate and body/substrate materials in chemical sensing applications [38, 39]. Similar to chemoresistors, these materials can suffer from severe degradation when being exposed to the atmosphere or interacting with analytes. A strong current decrease associated with continuous DC bias is also observed [40, 41], suggesting that introducing an off-state to relieve device stress during the measurement cycle is preferable.

The variations of V_T, in the mV range, can be either characterized directly by means of a gate-source voltage (V_{GS}) measurement at a constant drain-source current (I_{DS}) bias in the saturation region or indirectly through the change in I_{DS} at constant V_{GS} and drain-source voltage (V_{DS}). Normally, the former method is preferred since V_{GS} varies linearly with V_T. Although the I_{DS}-V_{GS} relation is nonlinear, ChemFETs can provide extra gain if they follow the conventional MOSFET I_{DS}-V_{GS} relationship. Assuming operation in the saturation region, the amplification factors in strong and weak inversion regions are given in (2.3) and (2.4), respectively:

$$\left.\frac{\Delta I_{DS}}{I_{DS}}\right|_{Strong}^{Const.V} = -\frac{2V_{GS}}{V_{GS} - V_T}\left.\frac{\Delta V_{GS}}{V_{GS}}\right|_{Strong}^{Const.I} \tag{2.3}$$

$$\left.\frac{\Delta I_{DS}}{I_{DS}}\right|_{Weak}^{Const.V} = -\frac{V_{GS}}{nkT/q}\left.\frac{\Delta V_{GS}}{V_{GS}}\right|_{Weak}^{Const.I} \tag{2.4}$$

where k is the Boltzmann constant, T is the absolute temperature, and n is the MOSFET subthreshold factor. While ChemFETs are based on the concepts of MOSFETs, they sometimes operate at voltages incompatible with CMOS circuits. As an example, the work function of specialized gate/substrate sensing materials may locate the ChemFET V_T beyond the normal V_T (<0.8V) found in sub-micron CMOS processes [42, 43]. Unlike CMOS processes, adjusting V_T by modifying channel doping level with ion-implantation may not be applicable to ChemFETs. Hence, ChemFETs may require a supply voltage higher than the nominal operating voltage of a specific CMOS process and the system power source, e.g., <3.6V for lithium-ion batteries or 1.5-3V for button cells. To improve the capability of the interface circuits, the designer may consider implementing an on-chip charge pump or a DC-DC boost converter. In terms of I_{DS}, ChemFETs are often operated in the low μA range or below. Not only is low-power electronics a trend, but also the Joule heating associated with higher currents may cause permanent damage to the ChemFETs.

2.1.4 Interface Circuit Specifications

So far, types of impedimetric electrochemical sensors and their characteristics have been introduced. Based on information gathered from multiple review papers [17, 20, 22, 25, 31, 38, 39, 44-50], Table 2.1 summarizes sensor baseline impedance ranges, ChemFET bias ranges, sensor response ranges, and some specific issues to be considered in interface design.

The next step is to compile interface specifications according to the information given in Table 2.1. Clearly, three-terminal ChemFETs exhibit significant fundamental

differences compared to two-terminal passive impedimetric sensors. The final approach is to implement two systems: one system deals with passive sensors, called the passive sensor interface in the following, while the other is dedicated to active sensors, called ChemFET interface. Table 2.2 and Table 2.3 list all specifications to be achieved in the passive sensor interface and the ChemFET interface, respectively.

Table 2.1: Summary of impedimetric sensor charateristics.

Chemical Sensor		Nominal Baseline/ Bias Condition	Nominal Sensitivity	Other Issue
Chemoresistor	MOx	10kΩ - 100MΩ	-1 to -4 decades	1/f noise
	CP (semiconductive)	>100kΩ	±10% to ±3 decades	Polarization effect 1/f noise
	CP (metallic)	100Ω - 100kΩ	< ±10%	Polarization effect 1/f noise
	Nanomaterial	10kΩ - 100MΩ	±10% to ±3 decades	1/f noise
Chemo-capacitor	Polymer	1pF - 100pF	< ±10%	
	Emerging Materials	1pF - 100pF	< 1000%	
ChemFET	General ChemFET	I_{DS} up to 10μA V_{GS} up to 10V V_{DS} up to 15V	$\Delta I_{DS} \approx \pm 1\%$ $\Delta V_T \approx \pm 10mV$	DC stress

Beginning from the top level, the upmost goal of this thesis is a low-power chemical sensing system operated by a battery. Among the variety of batteries, non-rechargeable lithium button cells demonstrate superior self-discharge rate and energy density. Ideally, a 3V-1000mAh coin cell [51] can provide continuous power to an 114μW system for 3 years, and hence an average power consumption of <100μW is desirable. The second important specification associated with chemical sensing is data readout pe-

riod, which is normally considered to be in the range of seconds since chemical sensors react with analytes at slow speed, i.e., time constant from seconds to minutes. Thus, an output data rate of 1Hz is sufficient. Both system specifications determined so far are applicable to both passive sensor interface and ChemFET interface.

By merging the nominal baseline resistance and sensitivity of the listed chemoresistors, it can be found that a suitable passive sensor interface should accommodate resistances from 100Ω to 100MΩ and provide 1% accuracy to resolve nominal <10% responses, corresponding to a 1% linearity as well as at least 40dB signal-to-noise ratio (SNR). The required dynamic range (DR) equals to 160dB. Here, the dynamic range, DR, is introduced to evaluate the performance of resistance and capacitance measurement circuits according to the definition published in the literatures [52]:

$$\mathrm{DR} = 20\mathrm{Log}_{10}\frac{\text{Measurement Range}}{\text{Full Range Linearity}}(\mathrm{dB}) \tag{2.5}$$

under the condition that SNR, which includes the quantization noise that limit the resolution, should be better than linearity across the full measurement range. For instance, an interface achieving 1% linearity in a specific range should also satisfy an SNR larger than 40dB. One should not mix up this definition with signal-to-noise dynamic range (SNDR) used to assess ADC performance. In fact, DR is a parameter that incorporates partial information of resolution, integral non-linearity (INL), and relaxed SNR in ADCs. Besides the DR, electronic circuits provide possible solutions to issues of aforementioned polarization effect and commonly observed high flicker noise (1/f noise) [53]. Regarding the capacitance DR, because the signal strength varies dramatically with different sensing materials, the accuracy is kept at 1% while the upper measurement limit should be extended 10 times beyond the baseline capacitance (1pF - 1nF), resulting in a DR of 100dB.

Table 2.2: Target specifications for the passive sensor interface.

Power Consumption	<100μW
Readout Speed	~1Hz
Resistance DR	160dB (100Ω - 100MΩ, 1% Linearity)
Capacitance DR	100dB (1pF - 1nF, 1% Linearity)
SNR	40dB
Special Issues	Reduce sensor 1/f noise Reduce polarization effect

The ChemFET interface has few challenges if it is designed exclusively for ISFETs, because ISFETs are fully compatible with CMOS processes in terms of manufacturing and operating voltages. However, a generalized ChemFET interface should demonstrate ability to generate high V_{GS} and V_{DS} biases. Expect for the additional power and readout requirements, specifications in Table 2.3 are exactly the same as the last row of Table 2.1.

Table 2.3: Target specifications for the ChemFET interface.

Power Consumption	<100μW
Readout Speed	~1Hz
I_{DS}	Up to 10μA
V_{GS}	Up to 10V
V_{DS}	Up to 15V
Noise Level	ΔI_{DS} = 1% ΔV_T = 10mV
Special Issue	Bias stress

2.2 Integrated Interfacing Techniques

Although the history of impedimetric chemical sensors can be traced back to the 1960s, it wasn't until the 1990s that people began paying attention to the integration of interface circuits [54, 55]. The reason is the relatively late maturity of integrated circuit

technologies and the recently increasing desire for stand-alone SoC sensor systems for environment monitoring and bio-chemical applications. The sub-chapter summarizes an exhausted literature survey of state-of-the-art integrated interfacing techniques for impedimetric sensors. Similar to Chapter 2.1, interfaces for chemoresistors, chemocapacitors, and ChemFETs are discussed separately. Multi-functional interfaces that measure resistance and capacitance simultaneously are discussed independently in Chapter 2.2.3.

2.2.1 Chemoresistor Interfaces

Before dedicated integrated interfaces for chemoresistors were proposed, researchers simply substituted resistor(s) in a voltage divider or a Wheatstone bridge (Figure 2.5) with chemoresistor(s) and measured the change of the output voltage V_O, which is related to sensor responses, i.e., the resistance change ΔR [56, 57]. However, this approach is rarely used today because the intrinsic non-linear relation between V_O and ΔR leads to a significant linearity error when ΔR is much greater than a few percent with respect to the baseline resistance.

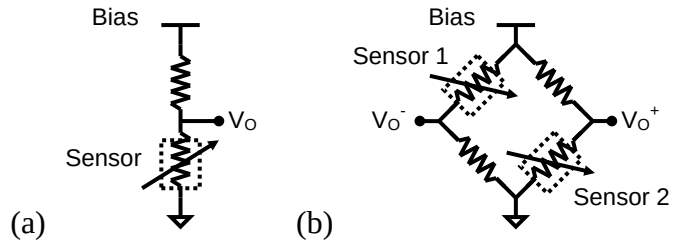


Figure 2.5: Basic interfaces for chemoresistors: (a) Voltage divider (b) Wheatstone bridge.

In terms of integrated circuit approaches, all published chemoresistor interfaces can be classified into two groups: direct measurement circuits and resistance-controlled oscillators (RCO).

In direct measurement circuits, a current voltage, I-V, measurement is used to extract either the V-R or I-R relationship based on Ohm's law. Either a test current I_{REF} or a test voltage V_{REF} is applied across the chemoresistor and the resistance values are obtained by measuring either output voltage V_{SEN} or current I_{SEN}, respectively. In 1994, Kordas, *et al.* demonstrated a topology similar to a four-wire measurement [58]: a V_{SEN} produced by a reference current I_{REF} flowing through a conductive sensing material is sampled with a capacitor and then amplified by a switched-capacitor (SC) amplifier. A few years later, Cardinali, *et al.* employed a continuous-time delta-sigma modulator (DSM) to integrate (sigma) the difference between sensor signal I_{SEN}, generated by V_{REF}, and reference current sources (delta) [59]. Additionally, compensation for humidity and alcohol are also implemented in this system; this is accomplished by weighing the integration factor of the DSM with bitstream-modulated duty-cycles and summing data from multiple sensors with an interleaving adder and a digital accumulator. An on-chip 4×4 MOx sensor array with simple front-end circuitry was proposed by Guo, *et al.* [60]. Each sensor is tested with an I_{REF} and differentially biased in the middle of positive and negative supply.

To expand the resistance measurement range, Barrettino, *et al.* and Ng, *et al.* took advantage of the logarithmic relation between voltage and current in a p-n junction diode to compress the voltages generated by I_{SEN} [61, 62]. Besides the readout circuitry, the former work includes a fully-integrated sensor array system including MOx sensors with

heating controllers, ADCs, and a digital I^2C interface; the later work includes a MOx sensor array and a spike pattern generator. While the logarithmic compression increases the measurement ranges, a linear measurement is still more preferable in terms of resolution and linearity. Grassi, *et al.* realized a 160dB DR (0.1% accuracy within 5 decades) linear measurement system based on I_{SEN} readout [52]. However, because I_{SEN} is not logarithmically compressed and the chip supply is limited, the 5-decade measurement range is divided into 10 sub-ranges with a programmable transimpedance amplifier controlled by a digital-to-analog converter (DAC) and a programmable resistor array. Moreover, to achieve continuity and reduce gain error between each sub-range, calibrations have to be performed and stored, then converted into analog currents through a DAC and a resistor bank before taking measurements.

When low power is the major concern, switched-capacitor (SC) circuits are first choice because of their low-energy charge-based signal conversion. Cho, *et al.* designed an I_{REF}-V_{SEN} topology for CNT gas sensors that is followed by a SC successive approximation (SAR) ADC optimized for conversion efficiency and consumes only 32μW [63]. This system achieves 97dB DR within 8 sub-ranges after calibrations.

Besides DR and power consumption, some research groups address other practical issues of chemoresistors, such as polarization effects and long-term drift, in their research. For certain chemoresistors, the long-term drift can exceed the responses caused by the analytes and, thus, can lead to fault detection. A possible solution proposed by Mu, *et al.* is to periodically track and remove the baseline resistance [64]. At the cost of 22 sub-ranges spanning 60kΩ to 10MΩ, they can attain 125ppm resolution in each sub-range, but their full-range linearity is not reported. Regarding the mitigation of po-

larization effects, Garcia-Guzman, *et al.* applied bipolar I_{REF} pulses to the chemoresistors and demonstrated a ratiometric readout topology to cancel out the long-term drift resulting from the material degradation and temperature variation [65]. Thereby, the testing I_{REF} that flows into the sensor is generated by applying V_{REF} across an inactive reference sensor made up of same sensing material, generating a ratiometric output between the sensor and the reference. They showed only simulation results of circuit together with well-modeled chemoresistors. D'Amico, *et al.* implemented an on-chip lock-in amplifier to improve the system sensitivity [66], because of its ability to recover tiny signals in a noisy environment. The restriction that lock-in amplifiers only accept sinusoidal signals is not merely negative. In fact, this enforcement of applying sinusoidal excitations to chemoresistors will also reduce polarization effects.

Table 2.4 and Table 2.5 summarize discussed chemoresistor interfaces using the direct measurement configuration, categorized by I_{REF} and V_{REF} stimulations, respectively. Different topologies are depicted in simplified system blocks. Important parameters, including measurable resistance range, linearity or resolution, power consumption, and output signal format are listed. If the full measurement range and either the full-range linearity or the resolution are available, the DR of the system is evaluated. It can be seen that high DR and/or low power consumption can be achieved in some topologies at the expense of a large number of sub-ranges. However, without calibrations to correct offsets and gain errors between each sub-range, device mismatch and process variation could be catastrophic to the full-range linearity. Although range division is often found in wide DR systems such as hand-held multi-meters, it is not friendly to integrated circuit (IC) systems that target mass production because of the above reasons. Generally, the amount of

cost and work increases with increasing number of sub-ranges.

Table 2.4: Summary of direct measurement interfaces with I_{REF} stimulation.

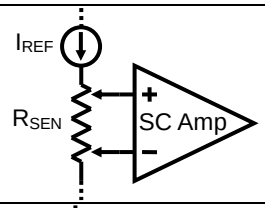
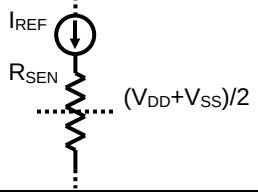
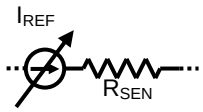
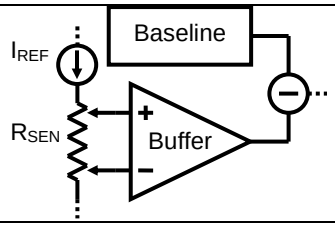
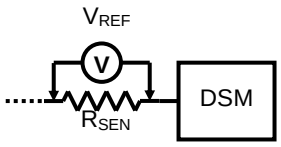
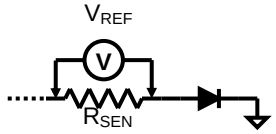
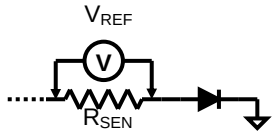
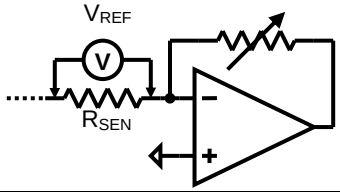
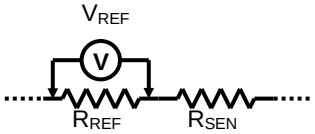
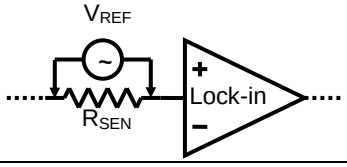
Literature	Topology	Resistance Range and Linearity	Power	Output Format
Kordas, *et al.* [58]		0.02 - 100mS/cm (N/A sub-ranges) ±1% Linearity (per sub-range)	10mW	Analog
Guo, *et al.* [60]		Up to 20MΩ (3 sub-ranges)	N/A	Analog
Cho, *et al.* [63]		10kΩ - 9MΩ (8 sub-ranges) ±1.34% Linearity (full range) DR = 97dB	32µW	Digital
Mu, *et al.* [64]		60kΩ - 10MΩ (22 sub-ranges) ±125ppm Linearity (per sub-range)	78µW	Analog

Table 2.5: Summary of direct measurement interfaces with V_{REF} stimulation.

Literature	Topology	Resistance Range and Linearity	Power	Output Format
Cardinali, *et al.* [59]		N/A	N/A	Pulse Density
Barrettino, *et al.* [61]		1kΩ - 10MΩ (single range) 10 bits Resolution (full range) DR = 60dB	N/A	Digital
Ng, *et al.* [62]		N/A	N/A	Digital
Grassi, *et al.* [52]		100Ω - 20MΩ (10 sub-ranges) ±0.1% Linearity (full range) DR = 166dB	6mW	Digital
Garcia-Guzman, *et al.* [65] (simulation)		N/A	N/A	Analog
D'Amico, *et al.* [66]		N/A	3mW	Analog

The RCO is an oscillator whose clock frequency depends on resistance values. The most significant benefit of representing resistance in the frequency domain is to circumvent the DR limitation caused by the supply voltage in I_{REF} stimulation cases and, thus, reduce the number of sub-ranges needed. As a result, RCOs are particularly attractive in wide DR circuit design. Another advantage of RCOs is their semi-digital output (i.e., digital clock); however, a counter and a highly stable time reference are necessary to

perform full digitization. RCOs originally evolved from the topology of V_{REF} stimulated direct measurement. Rather than measuring the current directly, I_{SEN} is taken by a relaxation oscillator or a ring oscillator to determine their oscillation time constant. The relaxation oscillator integrates I_{SEN} and resets at a specific level periodically; the ring oscillator integrates a decayed I_{SEN} to change the state of its inverting stages periodically. In simple terms, the chemoresistor is utilized to change the RC time constant of an oscillators.

Merino, *et al.* implemented an RCO interface by introducing a resistor-controlled delay stage into a ring oscillator [67]. The delay stage is simply an RC delay made up of a chemoresistor and a fixed capacitor.

The operation principle of RCO interfaces utilizing a relaxation oscillator topology is briefly discussed in the following. A V_{REF} is applied to the chemoresistor to generate a resistance-dependent I_{SEN}. I_{SEN} is then integrated by a fixed capacitor C_T to produce a ramping voltage whose slew rate is the ratio of I_{SEN} and C_T. A fixed reset level V_{RST} or hysteresis window V_{HYS} defined by designers determines when the integration is reset or reversed. It can be shown that, for a general relaxation oscillator, the oscillation period τ_{OSC} is proportional to the (chemo)resistor values if the comparator delay is assumed to be negligible:

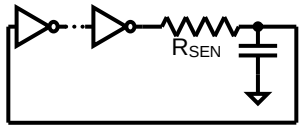
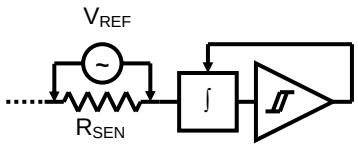
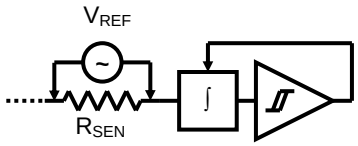
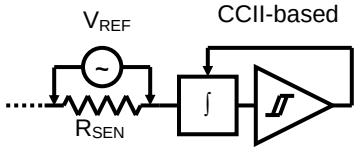
$$\tau_{OSC} = 2\frac{C_T V_{HYS}}{I_{SEN}} = 2\frac{R_{SEN} C_T V_{HYS}}{V_{REF}} \text{ or } = \frac{C_T V_{RST}}{I_{SEN}} = \frac{R_{SEN} C_T V_{RST}}{V_{REF}} \propto R_{SEN} \quad (2.6)$$

Grassi, *et al.* built a RCO based on the relaxation oscillator topology with an operation amplifier (OPA)-based integrator, current mirrors, and comparators [68]. After calibration, their system achieves 168dB DR within 3 sub-ranges. Grassi's architecture was later replicated by Bagga, *et al.* in a sensing system comprising an on-chip SnO_2 sensor, a relaxation-oscillator-based heater driver, and a RCO interface [69]. The RCO in Bagga's system

is a simplified version compared to Grassi's design. Besides using a regular OPA and comparator, Ferri, *et al.* demonstrated that all functions in a traditional relaxation oscillator can be realized with a single fundamental block, a second generation current conveyor (CCII) [70]. They only show simulation results of the integrated system, while the circuit functionality is verified with a PCB prototype.

Similar to Table 2.4 and 2.5, Table 2.6 summarizes different topologies of RCO-based interfaces and their respective performances. In comparison to direct measurements, RCOs easily reach 100dB DR because frequency has an ideally infinite DR, if the observation time is unlimited and clock jitter is kept sufficiently low. However, RCOs are usually power hungry, which is due to their high oscillation frequency and large V_{REF} induced I_{SEN} at low resistance levels.

Table 2.6: Summary of RCO interfaces.

Literature	Topology	Resistance Range and Linearity	Power Consumption
Merino, *et al.* [67]		10kΩ - 200MΩ (2 sub-ranges) ±1% Linearity (per sub-range)	N/A
Grassi, *et al.* [68]		1kΩ - 100MΩ (full range) ±0.8% Linearity (full-range) DR = 142dB 1kΩ - 1GΩ (3 sub-ranges) ±0.4% Linearity (full-range) DR = 163dB	15mW
Bagga, *et al.* [69]		50kΩ - 3.3MΩ (full-range) ±1.5% Linearity (full-range) DR = 73dB	N/A
Ferri, *et al.* [70] (simulation)		10kΩ - 100MΩ (full-range) ±0.8% Linearity (full-range) DR = 122dB	700μW

2.2.2 Chemocapacitor Interfaces

The pico-Farad baseline capacitance and femto-Farad response of chemocapacitors lie in the range that CMOS circuitry can easily handle. Compared to the chemoresistor interfaces in the previous sub-chapter, chemocapacitor readout circuitry encounters fewer challenges. Hence, rather than researching stand-alone chemocapacitor interfaces, most circuits were published in articles focusing on sensor design. Because capacitive humidity sensors have been proposed in the 1980s [31], chemocapacitor interfacing techniques are mostly found in 20 year old literature. Interestingly, very few cir-

cuits were published after 2000s.

According to its definition, capacitance can be evaluated by the amount of charge being held per unit voltage across a capacitor. Designers can hence consider taking advantage of SC amplifiers. Charge redistribution amplifiers, a slight variation of SC amplifiers, have long been a popular circuit for capacitance to voltage conversion. Dura, *et al.* and Qiu, *et al.* utilized similar charge redistribution amplifiers in monolithic humidity sensing systems to measure the capacitance difference between the sensor C_{SEN} and a reference C_{REF} [71, 72]. Their architecture is essentially a two-input SC summation amplifier. Instead of summing input voltages, the sensor and the reference serve as input weighting capacitors that determine different gains to corresponding fixed input voltages. When C_{SEN} and C_{REF} take turn to be fully charged and discharged in the same clock phase, the common mode charges will exchange between C_{SEN} and C_{REF} and only the difference charges will be forced into a feedback capacitor C_{FB}. Assuming an ideal OPA, the output voltage V_{OUT} of the charge redistribution amplifier is governed by the following equation:

$$V_{OUT} = \pm V_{\alpha} \frac{C_{SEN}}{C_{FB}} \mp V_{\beta} \frac{C_{REF}}{C_{FB}} \tag{2.7}$$

where V_{α} and V_{β} are DC voltages applied to C_{SEN} and C_{REF} inputs, respectively. The polarity in the equation depends on the timing of sampling or resetting, i.e., within either one of the clock phase. Dura's design was a basic version with same the V_{α} and V_{β}; Qiu enhanced the amplifier with a low-pass feature and left V_{α} and V_{β} tunable to compensate for offsets in the OPA and initial mismatch between C_{SEN} and C_{REF}.

As the frequency of RCOs relies on an RC time constant, a counterpart called capacitance-controlled oscillators (CCOs) can also be realized in either a relaxation oscillator or ring oscillator architecture. Baltes, *et al.* integrated a polysilicon-polysilicon capac-

itive humidity sensor into a relaxation CCO using a CMOS process [73]. Comparing their CCO with equation (2.6), C_T is replaced by C_{SEN} and I_{SEN} becomes an on-chip constant current source I_T. Consequently, τ_{OSC} can be shown to be proportional to C_{SEN}:

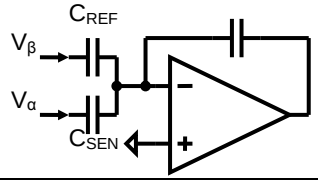
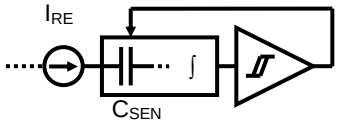
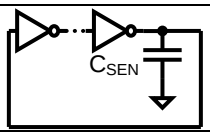
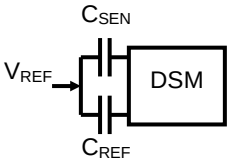
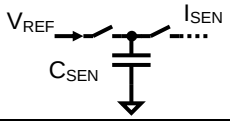
$$\tau_{OSC} = 2\frac{C_{SEN}V_{HYS}}{I_T} \propto C_{SEN} \tag{2.8}$$

Yang, *et al.* considered the humidity sensor as an additional capacitive load in a ring oscillator that increases and modulates the gate delay, resulting in a change of the oscillation frequency [74].

The possibility to leverage DSM for capacitance readout has also been explored. A discrete-time DSM has a SC integrator input stage whose sampling capacitor can be substituted with C_{SEN}. Sampling a fixed input voltage with C_{SEN} is similar to sampling a variable input voltage with a fixed capacitor in the delta-sigma ADC case, both resulting in a variation in the sampling charges. Cardinali, *et al.* and Cornila, *et al.* successfully combined chemocapacitor with DSMs [59, 75]. The former is a single-ended topology and the latter is a fully-differential DSM; nevertheless, both circuits can measure the difference between the C_{SEN} and a C_{REF}. Sometimes, it is desirable to measure absolute capacitance value, which is achievable with a SC resistor emulator. SC resistor emulators have an equivalent resistance of 1/fC, where f is the switching frequency and C is the capacitance. By applying a fixed voltage and measuring the current, capacitance can be determined. Boltshauser, *et al.* employed this concept by switching a capacitive humidity sensor and measuring the average current of the sensor [76].

Table 2.7 summarizes the discussed interface circuits for chemocapacitors. As mentioned before, chemocapacitor interfaces are usually not a stand-alone research topic and thus, independent circuit performances are not reported in most literatures.

Table 2.7: Summary of chemocapacitor interfacing techniques.

Literature	Topology	Output
Dura, *et al.* [71] Qiu, *et al.* [72]		Analog Voltage
Baltes, *et al.* [73]		Digital Clock
Yang, *et al.* [74]		Digital Clock
Cardinali, *et al.* [59] Cornila, *et al.* [75]		Pulse Density
Boltshauser, *et al.* [76]		Analog Current

2.2.3 Multi-functional Interfaces and Impedance Spectroscopies

Multi-functional interfaces and impedance spectroscopy refer to circuitry that is able to measure resistance and reactance of sensors with a single circuit architecture. In practice, large inductance suitable for low frequency sensing applications is not easily realized with micro-fabrication technologies and, thus, inductive chemical sensors and their interfaces are seldom found. Ferri, *et al.*, modified an RCO-based chemoresistor interface, which was originally designed for large DR applications, to measure the parallel capacitance of the sensors [77, 78]. The working principle of their circuit is shown in Figure 2.6: the chemical sensor and a parasitic parallel capacitor C_{PAR} are excited simultaneously with a square wave V_{EX} generated by the feedback signal generated from the

output of a hysteresis comparator. Because the non-zero C_{PAR} causes a rapid charge injection into the feedback capacitor C_{FB}, the integrator output V_{INT} becomes a superposition of triangular and square waves. Intuitively, it can be view as a two-input summation amplifier: one input for integration and the other for amplification. As V_{INT} is limited by the hysteresis voltage V_{HYT}, the additional up and down steps force a change in the oscillation period. V_{INT} is further compared to a fixed level and, using some logics, converted into a V_{DT} pulse whose period and duty-cycle are related to R_{SEN} and C_{PAR} through rather complicated equations. Ferri's circuit was published in two versions in 2009 [77] and 2013 [78]. The earlier one consumes 4mW and exhibits a resistance DR of 141dB (1% linearity from 470kΩ to 50GΩ) and a capacitance DR of 41dB (0.3pF accuracy from 0pF to 33pF); the more recent version consumes less power (600μW) but shows a lower resistance DR of 80dB (10% linearity from 100kΩ to 100MΩ) and a 10% capacitance accuracy in the range of 0pF to 22pF.

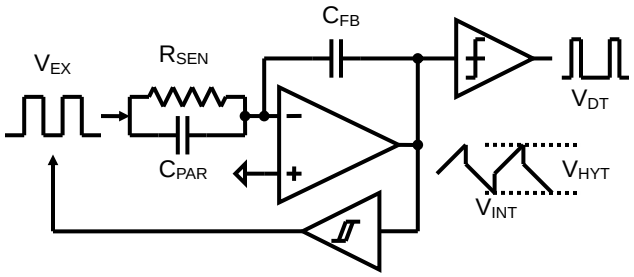


Figure 2.6: System diagram of modified RCO for parallel capacitance extraction [77].

Impedance spectroscopy uses part of the lock-in amplifier architecture to acquire the real and the imaginary parts of an unknown impedance. The fundamental principle is based on the multiplication of the original excitation and the sensor signal I_{SEN} to down

convert the real and imaginary part of the impedance to DC levels. A chemical sensor exhibiting an impedance Z is driven by a sinusoidal AC voltage Asin(ωt) with amplitude A at a given frequency ω to generate a sensor current I_{SEN} = Asin(ωt - θ)/|Z| at the same frequency with a phase shift θ. I_{SEN} is then multiplied by a square wave in phase with the excitation signal and integrated (and filtered) over several periods to obtain the real part of the impedance. If I_{SEN} is multiplied by a 90-degree phase-shifted square wave, the output will be the imaginary part of the impedance. Mathematically, the results of both multiplications are expressed in equations 2.9 and 2.10, where Z = R + jX denotes the sensor impedance and N is the number of integration cycle:

$$\int_0^{\frac{2N\pi}{\omega}} \frac{A\sin(\omega t-\theta)}{|Z|}\frac{\pi}{4}\sum_{k=1}^{\infty}\frac{\sin((2k-1)\omega t)}{(2k-1)}dt = \frac{4AN}{\omega|Z|}\cos(\theta) = \frac{4AN}{\omega}\frac{R}{|Z|^2} \tag{2.9}$$

$$\int_0^{\frac{2N\pi}{\omega}} \frac{A\sin(\omega t-\theta)}{|Z|}\frac{\pi}{4}\sum_{k=1}^{\infty}\frac{\sin((2k-1)\omega t-\frac{\pi}{2})}{(2k-1)}dt = \frac{4AN}{\omega|Z|}\sin(\theta) = \frac{4AN}{\omega}\frac{X}{|Z|^2} \tag{2.10}$$

Manickam, *et al.* and Yang, *et al.* implemented integrated impedance spectroscopy circuits for biosensor arrays [79, 80]. Manickam's circuit, shown in Figure 2.7(a), consists of a traditional lock-in stage followed by a low-pass filter (LPF). The LPF is used to remove the harmonics generated by the multiplication, which should give sufficient suppression to signal frequency down to ω, the first harmonic. The system allows sensing currents I_{SEN} from 330pA to 25μA, corresponding to 97dB DR, at 10Hz bandwidth. The power consumption is 848μW per pixel in a 10×10 on-chip sensor array. Shown in Figure 2.7(b), Yang's circuit has a pseudo-DSM after the multiplier and a counter to serve as a moving average filter for decimation. The DSM can reduce noise the level by integrating and oversampling I_{SEN}. Their system can accept I_{SEN} from 78fA to 100nA within 3

sub-ranges, but the full-range linearity is not provided. The power consumption is only 6μW.

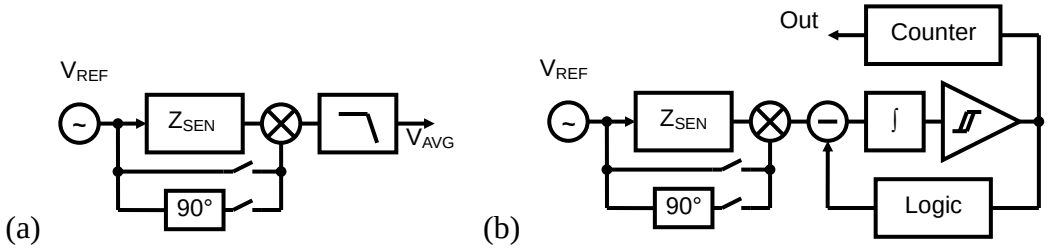


Figure 2.7: System diagrams of two lock-in impedance spectroscopy systems (a) using conventional LPF [79] and (b) employing first-order DSM [80].

Murali, *et al.* proposed an unconventional impedance spectroscopy circuit using an on-chip DSM and external DSP for conductive polymer sensor arrays [81]. Their system is designed to measure the impedance ratio between a sensor, a Wheatstone bridge consisting of two diagonally arranged chemoresistors and two traditional resistors, and a reference pixel (resistor) containing an inactive sensor. Both sensors and reference are driven by an AC signal up to 10kHz and the output currents are fed into several amplifier and DSM stages right next to each pixel. The bitstreams of the DSM are processed by off-chip fast Fourier transform (FFT) DSP followed by additional computation to extract the relative impedance between sensors and reference. The system provides a DR of 48.9dB and consumes 1.9mW in each pixel.

The advantage of impedance spectroscopy is its ability to analyze impedance as a function of frequency. However, it requires a variable frequency driver with a clean spectrum and a well-controlled amplitude and, thus, [79-81] typically relies on external high-performance signal generators as excitation sources. Reviewing (2.9) and (2.10),

any harmonics in I_{SEN}, caused by the driving signal, results in additional DC components that degrade the linearity of the outputs. If circuit complexity and power consumption are not major concerns, on-chip AC signal generators such as direct digital synthesizers (DDS) and phase lock loops (PLL), could be a solution.

2.2.4 Chemical Field-Effect Transistor (ChemFET) Interfaces

A significant amount of effort has been devoted to integrated ISFET interfaces, yet there is no publication proposing a generic interface circuit for ChemFETs. Although the literature search performed for this sub-chapter only yielded ISFET interfaces, the strategy is to discover common circuit techniques for FET-type sensors and leverage them in the proposed design. ISFET interfaces come in many variations, but most of them are based on three operation principles: constant current mode, constant voltage mode, and ISFET OPA, which are illustrated in Figure 2.8. The FET symbols with bold gate terminal denote the ISFETs; the gate of the ISFET is a floating electrode biased at V_{REF} and coupled through a liquid. V_D and V_S denote drain and source voltages, respectively.

In constant current mode (Figure 2.8(a)), I_{DS}, V_D, and V_{REF} are kept constant. The change in threshold voltage ΔV_T can be determined by measuring the source voltage V_S, as V_S changes equally but negatively with ΔV_T ($\Delta V_S = -\Delta V_T$). In constant voltage mode (Figure 2.8(b)), ΔV_T is measured indirectly through the change of I_{DS} when all terminals are given constant voltage biases. The ISFET OPA (Figure 2.8(c)) is essentially a constant current mode architecture in a differential configuration, realized by the differential input pair of an OPA comprising the ISFET and a normal reference ISFET (REFET). The negative feedback through a transimpedance stage forces the ISFET to bias at a constant

I_{DS} related to the tail current I_{REF}. ISFET OPAs have the advantage to reject common mode variations such as V_T and temperature drifts.

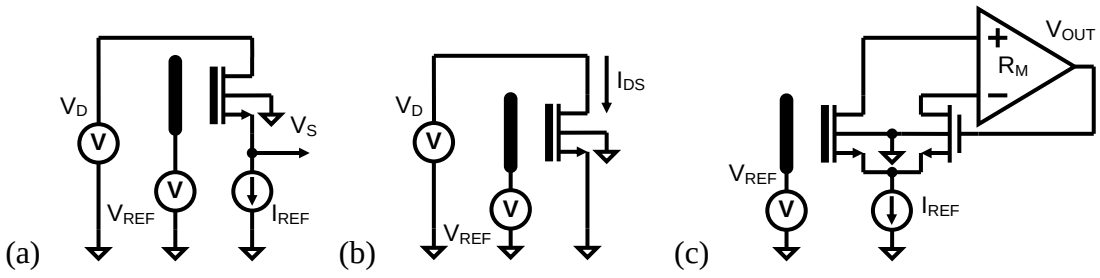


Figure 2.8: ISFET interface topologies: (a) constant current mode, (b) constant voltage mode, and (c) ISFET OPA.

Based on the topology in shown Figure 2.8(a), Tzukada, *et al.* integrated an ISFET array with on-chip buffers and multiplexers in the late 1980s [82]. In 1990s, Palan, *et al.* and Ravezzi, *et al.* improved Tzukada's topology by V_{DS} regulation to allow triode region operation [83, 84]. Palan implemented two identical circuits to perform a differential readout. Instead of reading V_S, Thanachayanont, *et al.* made slight modification to the current mode topology to measure the difference in channel resistance between ISFET and REFET and convert it into a current [85]; only simulation results were reported. For temperature compensation, Chung, *et al.* designed a V_T extractor and an external software-based algorithm to remove the temperature dependency of V_T [86, 87]. They also included an LCD driver and a calibration circuit in the same chip. P. K. Chan, *et al.* analyzed the ISFET temperature dependency and proposed an iteration method to find the athermal biasing point to minimize temperature effects [88]. The V_T in their circuit is measured in terms of V_{GS} through a self-biasing scheme which ties V_S to ground to reduce the body effect. W. P. Chan, *et al.* reduced ISFET noise by averaging signals of an

8×8 array and added a frequency domain DSM for digitalization [89]. A robust system consisting of memory, microcontroller unit (MCU), and an analog front-end circuit similar to Palan's design was presented by Hammond, *et al*. [90]

In constant voltage mode, Shepherd, *et al.* biased ISFETs in their subthreshold region [91]. The author derived the translinear relation between I_{DS} and pH level and verified it by simulation. Kalofonou, *et al.* utilized a Gilbert gain cell to realize a differential measurement and current output in the subthreshold region [92]. In Bausells', *et al.* and Chin's, *et al.* designs, ISFETs were biased with constant V_{DS} in the triode region to serve as V_T-controlled variable resistors. Then, the ISFETs were embedded into instrumentation amplifiers to modulate the gain and, hence, output voltage of the amplifier [93, 94]. Morgenshtein, *et al.* showed that the differential measurement of an ISFET/REFET pair can also be realized with a Wheatstone bridge in simulation results [95]. Besides, they demonstrated four possible configurations in constant current and constant voltage modes for n-type and p-type ISFETs [96]. One of these configurations was employed and implemented in a differential readout topology by Chodavarapu, *et al.* [97].

ISFET OP-Amps have been implemented because of their self-feedback, differential, and low output impedance advantages. In 1989, Wong, *et al.* proposed a scheme with two ISFET OPAs to show the signal difference between two ISFETs with heterogeneous gate coating materials, Ta_2O_5 (58-59mV/pH) and SiO_xN_y/Si_3N_4 (18-20mV/pH) [98]. A single ISFET OPA can mitigate temperature effects with a REFET counterpart, however, it still required an off-chip "ideal" reference electrode, normally an Ag/AgCl wire or a calomel electrode. Using an additional ISFET OPA, the authors relaxed the requirement for an ideal electrode and, thus, the counter electrode can be implemented on-chip with

an available Au/Cr noble metal. This differential difference topology achieved a 40-43mV/pH sensitivity and accomplished a fully integrated ISFET system. A single ISFET OPA was revisited and deeply studied by Neuzil to evaluate light effects [99]. A liquid imager was built by Goh, *et al.* with a two-dimensional ISFET OPA array [100]. The imager can provide fully digital outputs and perform self-calibration to remove initial pixel mismatch.

Not falling into the three previously discussed categories, a simple two-transistor inverting amplifier employing a p-type ISFET as the active load (i.e., ISFET current source) was proposed by Liu, *et al.* [101]. The amplifier is driven by a large-signal triangular wave, and thus the amplifier output is a square wave and ΔV_T is sensed indirectly through the change of the square wave duty cycle. A detail is that ΔV_T causes a change of the ISFET sourcing current and, thus, the switching level of the triangular wave and the output duty cycle.

The state-of-the-art ISFET interfaces and their respective features are summarized in Table 2.8. Although the literature search results did not yield any solution to the major challenge, namely high bias voltages, of a generic ChemFET interface, they suggest that operating ChemFETs in different modes or bias regions may provide benefits to a specific application. Consequently, in addition to the voltage range, expanding ChemFET interface versatility is seriously considered in the design.

Table 2.8: Summary of ChemFET interfaces.

Topology	Literature	System Feature
Constant Current Mode	Tzukada, *et al.* [82]	ISFET array Multiplexer
	Palan, *et al.* [83] Ravezzi, *et al.* [84]	Accurate V_{DS} regulation
	Thanachayanont, *et al.* [85] (simulation)	Differential output
	Chung, *et al.* [86,87]	Programmable bias current Temperature sensor Temperature calibration Dual-slope ADC LCD driver
	P. K. Chan, *et al.* [88]	Athermal I_{DS} biasing
	W. P. Chan, *et al.* [89]	8×8 ISFET array Frequency domain DSM
	Hammond, *et al.* [90]	Programmable bias current Differential output On-chip microcontroller
Constant Voltage Mode	Shepherd, *et al.* [91] (simulation)	Subthreshold operation
	Kalofonou, *et al.* [92]	Gilbert gain cell
	Bausells, *et al.* [93] Chin, *et al.* [94]	Triode operation
	Morgenshtein, *et al.*[95,96] (simulation)	Triode operation Wheatstone bridge ISFET inverter with OP-Amp feedback
	Chodavarapu, *et al.* [97]	ISFET inverter with OP-Amp feedback
ISFET OP-Amp	Wong, *et al.* [98]	Differential readout
	Neuzil [99]	Light effect measurement
	Goh, *et al.* [100]	ISFET array averaging Auto-calibration
Inverter	Liu, *et al.* [101]	Duty cycle output

CHAPTER 3

MICROFABRICATED IMPEDIMETRIC CHEMICAL SENSORS

This chapter introduces two in-house microfabricated chemical sensors: a multi-functional passive impedimetric sensor and an indium-gallium-zinc-oxide (IGZO) TFT ChemFET. The device structures, fabrication steps, and operation principles will be described in the following sub-sections. These sensors are ultimately interfaced with the proposed circuits. Thus, preliminary gas measurements were carried out in a customized gas-setup, which will be described in Chapter 6, using bench-top measurement equipment to verify sensor functionalities and establish design criteria for the interface circuits.

3.1 Multifunctional Passive Impedimetric Chemical Sensor

Like many chemical sensors, (room-temperature) impedimetric sensors are often limited in terms of their selectivity, i.e., their ability to distinguish between different analytes. One way to improve the analyte discrimination is to use higher-order sensing systems [102], e.g., a sensor array coated with different (partially selective) sensing films, so that the property change, e.g., conductivity, of multiple sensors upon analyte sorption forms a characteristic pattern to a specific analyte. Using proper pattern recognition algorithms, sensor selectivity can ultimately be improved. Alternatively (or in addition), different properties of the sensing films can be explored using multi-transducer arrays [11]. By using so-called multifunctional sensors, different properties of the same sensing films can be measured subsequently or simultaneously [103, 104]. As the title of this sub-chapter suggests, the present work aims at combining a chemoresistor and a

chemocapacitor in a single device structure. This way, depending on the particular sensing film, either resistive response, capacitive response, or both can be explored in a given application.

The electrode layout and the cross-section of the proposed multifunctional impedimetric sensor are shown in Figure 3.1. The sensor structure comprises a set of non-passivated interdigitated finger electrodes that serve as the two terminals of the resistive sensor. A third, passivated conductor meanders in-between the two finger electrodes and forms one electrode for the capacitive sensor. In resistance measurement mode, the coating resistance is measured using the non-passivated finger electrodes, while the meandering capacitive electrode is kept floating. In capacitance measurement mode, the two finger electrodes are shorted to each other and form the counter-electrode to the passivated electrode. If the system is properly designed, one can rapidly switch between the two measurement modes to improve analyte discrimination.

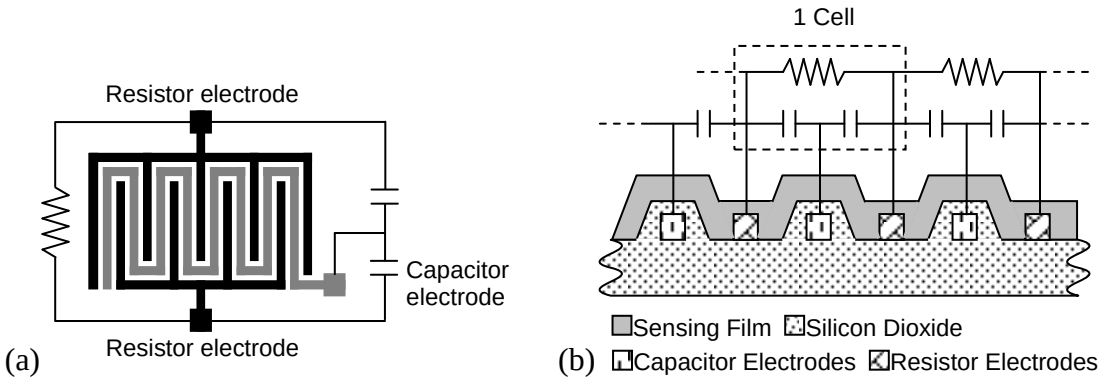


Figure 3.1: (a) Electrode layout and (b) cross-section of multifunctional passive impedimetric sensor.

Figure 3.2 shows a microscope image of a corner of the fabricated multifunctional sensor with two gold finger electrodes and the passivated third electrode meandering in-between. The impedimetric microsensors are fabricated using a three-mask process. The process flow begins with growing a layer of thermal oxide on a blank silicon wafer for isolation. Next, a 250nm thick gold layer is deposited, patterned and subsequently passivated using a PECVD silicon nitride film to form the meandering capacitor electrode. The pad regions are then opened and the nitride between neighboring metal lines is partially etched away under the condition that the sidewalls of the passivated capacitor electrodes are still protected by nitride. The purpose of this step is to allow the coated sensing film to nestle closer to the passivated electrode. Finally, another 250nm thick gold layer was deposited and patterned with lift-off process to form the interdigitated electrodes of the resistor contacts. While the devices tested in this work were fabricated in a dedicated process, similar structures can be easily embedded into the back-end metallization of a CMOS process.

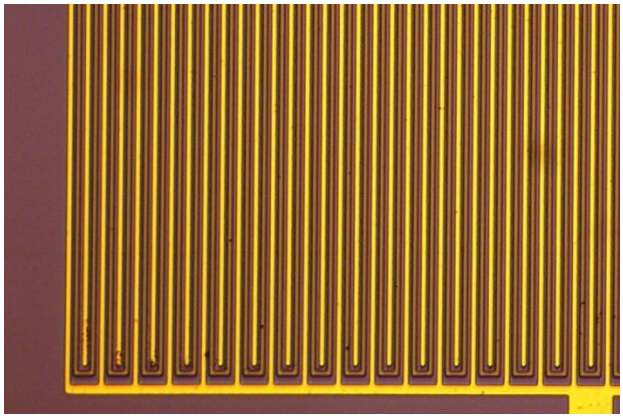


Figure 3.2: Microscope image of corner of microfabricated sensor.

On the same wafer, devices with different overall dimensions and electrode pitches were fabricated to investigate the effect of the device dimension on the chemical sensing performance. A $5\times5mm^2$ die typically houses eight square sensors with different sizes: two $2\times2mm^2$, two $1\times1mm^2$, and four $0.5\times0.5mm^2$ devices. Devices with electrode pitches from 3μm to 6μm are randomly distributed across the wafer. Chemoresistors and chemocapacitors (not multi-functional sensor) are also fabricated on the same wafer in a similar manner. The former is a structure without the meandering electrode; the latter is simply a passivated chemoresistor. After polymer coating, these dimensions typically result in baseline capacitances >10pF and film resistances ranging from few ~10Ω to ~100MΩ, strongly depending on the sensing film material.

In this work, the performance of resistive/capacitive multisensors coated with dielectric polyepichlorohydrin (PECH) and conductive poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS) (purchased from Sigma-Aldrich) sensing films was examined. Solid PECH was dissolved in gently heated (50℃) chloroform and spray-coated onto individual sensor chips, resulting in typical film thicknesses of 2μm. The PEDOT:PSS used in this work is dispersed in water, which makes evaporation too slow to distribute the polymer uniformly across the chip by spray coating. Thus, a simple drop coating technique was implemented which results in a uniform film coating of approx. 2μm.

Considering measurement flexibility and noise performance, the device resistance and capacitance were measured separately using a Keithley 2636A System Source Meter and an Agilent 4284A Precision LCR Meter, respectively. The capacitances were measured at a frequency of 10kHz. The measurement mode, either AC or DC, was found to

significantly affect the signal shape and device stability in the resistive measurement. Initially, resistive measurements were performed by sourcing a constant DC current and measuring the voltage drop across the sensor. It was found that the DC bias rapidly degrades the PEDOT:PSS coating conductivity, resulting in an approx. 20 times increase in the baseline resistance. It is speculated that polarization effects in the polymer cause this significant resistance change. To mitigate such polarization effects and improve the long-term stability, bipolar AC pulses with a 5% duty cycle were applied every second for all resistance measurement shown in the later sections.

Figure 3.3 compares the sensor responses of a PEDOT:PSS-coated device exposed to 1500, 3000, 4500, 6000, 6000, 4500, 3000, and 1500ppm of ethanol vapor at room temperature in case of continuous DC biasing (red line) and bipolar pulse biasing with a 5% duty cycle (blue line). The DC bias results in significantly higher baseline resistances and the sensor response changes signs with increasing analyte concentration. The AC biasing scheme stabilizes the baseline resistance and the sensor response increases with increasing analyte concentration. Interestingly, the characteristic time constants increase significantly in case of bipolar biasing.

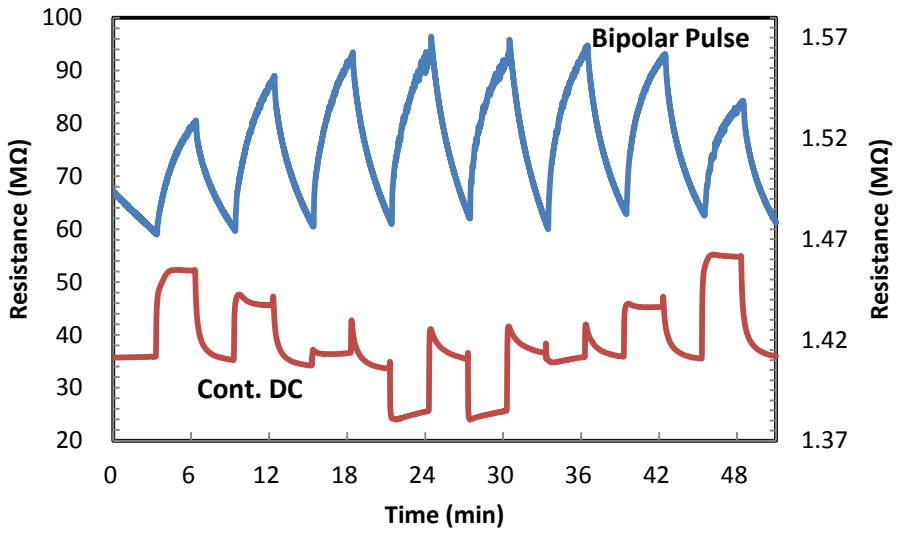


Figure 3.3: Comparison of resistive responses of PEDOT:PSS-coated sensors biased with bipolar pulses and continuous DC.

To verify the design, a capacitive mode measurement was first performed with a non-conductive polymer as a sensing film. To this end, a capacitive sensor with passivated interdigitated electrodes and a 3µm electrode pitch was spray-coated with a ~2µm thick non-conductive PECH film. A baseline capacitance of approx. 66.5pF was measured after removing package parasitic capacitances. Upon absorption of analytes, the change of the effective dielectric constant of the polymer and possible polymer swelling result in a measurable capacitance change. Two analytes, ethanol and toluene, were chosen to investigate effects of polar and non-polar analytes. Figure 3.4 displays the resulting capacitance change upon exposure to different analyte concentrations of ethanol (7500, 15000, 22500, and 30000ppm) and toluene (5125, 10250, 15375, and 20500ppm) at room temperature. After 3 minutes of each analyte exposure, the measurement chamber was flushed with synthetic air for 3 minutes as reference gas. As expected, ethanol shows a positive response while toluene shows a negative response, because the relative dielectric

constant of PECH ($\varepsilon_r \approx 7$-8) lies in-between the dielectric constants of toluene ($\varepsilon_r \approx 2.4$) and ethanol ($\varepsilon_r \approx 24.3$). The higher sensitivity for toluene can be explained by the higher partition coefficient for toluene in PECH ($K_{toluene} = 1370$, $K_{ethanol} = 117$ in PECH [105]).

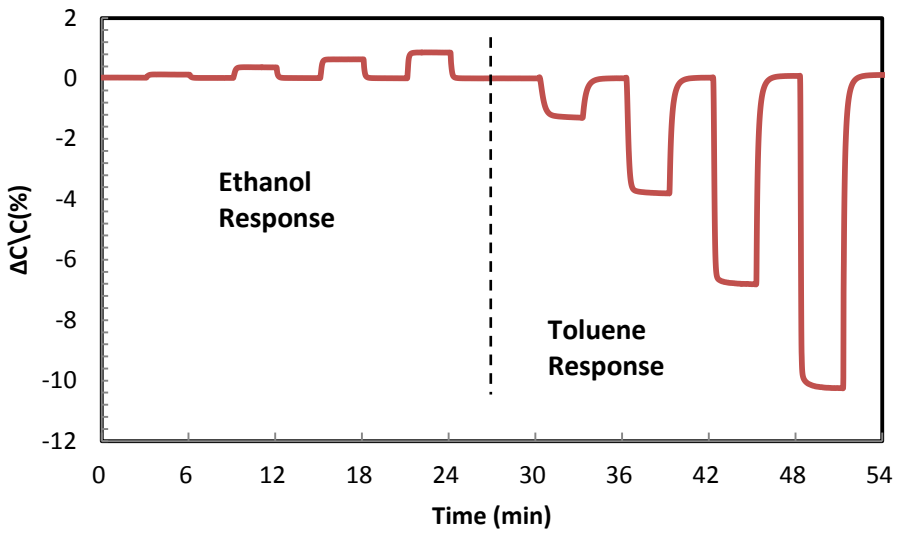


Figure 3.4: Relative capacitance change of sensor coated with ~2µm PECH upon ethanol and toluene exposure.

To test both operation modes of the transducer on a single sensing film, low-conductivity PEDOT:PSS (Sigma Aldrich, 2.8wt% dispersion in H_2O) was diluted 20 times and drop-coated onto a sensor structure, resulting in a ~2µm thick sensing layer. The baseline capacitance was measured to be 21pF and the baseline resistance was approx. 1.5MΩ. The resistance readout was extracted from the voltage drop across the device by applying ±1µA current pulses. Capacitance measurements were again taken at 10 kHz AC.

Figure 3.5 shows the response of the PEDOT:PSS-coated sensor operated in resistive mode, i.e., the relative change in resistance, upon exposure to different concentra-

tions of ethanol (1500, 3000, 4500, and 6000ppm) and isopropanol (600, 1200, 1800, and 2400ppm) at room temperature. In case of ethanol, we see a relatively strong sensor response compared to the capacitance response of a PECH-coated sensor in Figure 3.4, which might not be surprising as PEDOT:PSS is originally dissolved in water and, thus, the partition coefficients for polar alcohols might be high. Interestingly, the ethanol and isopropanol responses in Figure 3.5 show dramatically different time constants, with a short response time for the larger isopropanol molecule. It is speculated that the long time constants in case of ethanol may be due to a slow chemical reaction between the analyte and the polymer. This might also explain the poor signal linearity observed with ethanol, but additional measurements are needed for clarification. In the isopropanol case, the resistance change increases more linearly with the analyte concentration with relatively short signal transients.

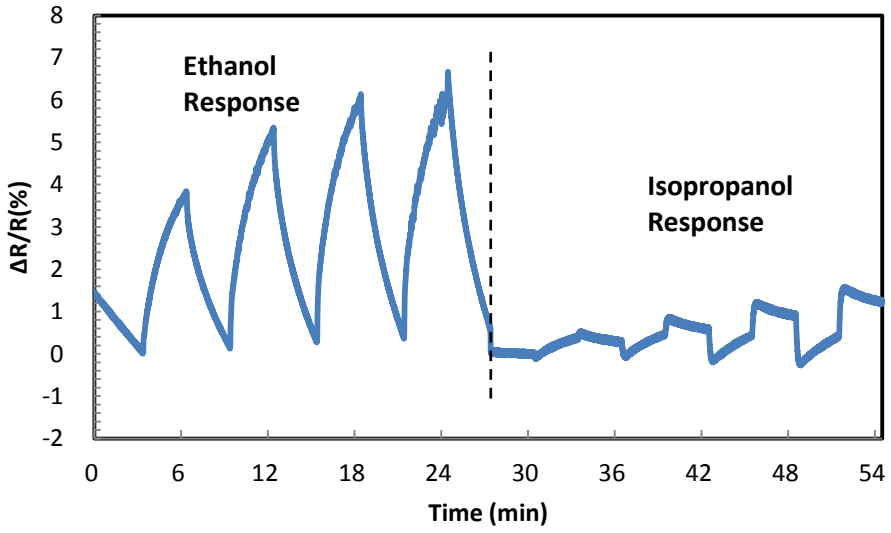


Figure 3.5: Relative resistance change of PEDOT:PSS-coated multifunctional sensor upon exposure to different concentrations of ethanol and isopropanol.

Figure 3.6 shows the response of the PEDOT:PSS-coated sensor operated in capacitive mode, i.e., the relative change in capacitance, upon exposure to different concentrations of isopropanol (600, 1200, 1800, and 2400ppm) and toluene (1025, 2050, 4100, and 8200ppm) at room temperature. Because the low-conductivity type PEDOT:PSS with a specified conductivity of 10^{-5}S/cm is far from being an ideal conductor, a considerable capacitive signal can actually be measured. For both analytes, positive capacitance changes are observed upon analyte sorption with short signal transients that are likely associated with the analyte diffusion into the polymer. In contrast to non-conducting polymers, such as PECH, the imaginary part of the complex permittivity plays an important role in the observed capacitive responses. The imaginary part of the complex permittivity $\hat{\varepsilon}$ increases linearly with the electrical conductivity:

$$\hat{\varepsilon} = \varepsilon' + i\frac{\sigma}{\omega} \tag{3.1}$$

where ε', σ, and ω are the real part of the permittivity, the conductivity, and the angular frequency, respectively. Thus, the imaginary part can dominate the capacitive response especially at relatively low probing frequencies, resulting in responses similar to resistance measurements. Hence, it suggests that probing device with high-frequency AC signal can improve the permittivity dependency on conductivity change.

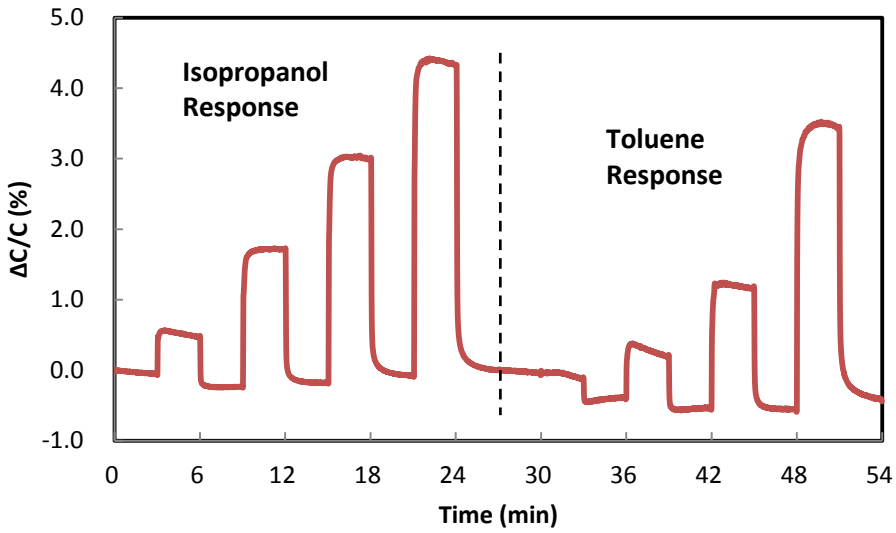


Figure 3.6: Relative capacitance change of PEDOT:PSS-coated device upon exposure to different concentrations of isopropanol and toluene.

3.2 Indium-Gallium-Zinc-Oxide Thin-Film Transistor Chemical Sensor

Thin-film transistors (TFTs) made from transparent oxide semiconductors have recently found their way into (bio-)chemical sensing applications [106, 107]. The indium gallium zinc oxide (InGaZnO) semiconductive film has received much attention for TFTs, due to the high saturation electron mobility (μ_{SAT} > 6cm^2/V-s), high on-off ratio (>10^6), and low leakage current that can be achieved, even when deposited at room temperature [108]. These attributes allow InGaZnO TFTs to take part in the emerging flexible substrate applications.

The fabricated InGaZnO TFTs are staggered, bottom-gate devices on 4" n-type Si wafers. In order to isolate each device, a 1µm thick thermal oxide layer was first grown. Bottom-gate electrodes made from electron-beam deposited aluminum were then patterned for individual control of each device across the wafer. A 50nm aluminum oxide (Al_2O_3) layer deposited via atomic layer deposition (ALD) at 180℃ was used as the gate

dielectric. Subsequently, RF sputtering from an InGaZnO (1:1:1) ceramic target was conducted at room temperature to deposit a 50nm thick active layer. Finally, chromium/gold drain and source contacts were created using lift-off.

It has been widely shown that InGaZnO TFTs suffer from constant bias stress instability that causes I_{DS} to decay, or on the other hand, V_T to increase exponentially over time [109, 110]. Consequently, a post-process annealing at 300℃ in air was performed for 90 minutes to improve the V_T stability of TFT. Figure 3.7 shows the cross-sectional view and the micrograph top-view of a TFT with 5µm channel length and wide-over-length ratio of 466.

The electrical performance of the TFTs can be extracted from the transfer characteristic (V_{GS} vs. I_{DS}) shown in Figure 3.8. The measurements were carried out in a sealed metal case at room temperature with a Keithley 2636A low-current dual-channel sourcemeter. A linear extrapolation of the square-root of I_{DS} as a function of V_{GS} in the saturation region (dashed line) shows that V_T is ~1.9V. Additionally, in the logarithmic scale, it is observed that the on/off ratio is $>10^7$, μ_{SAT} is $>4cm^2/V\text{-}s$, and the sub-threshold swing is 0.18V/dec.

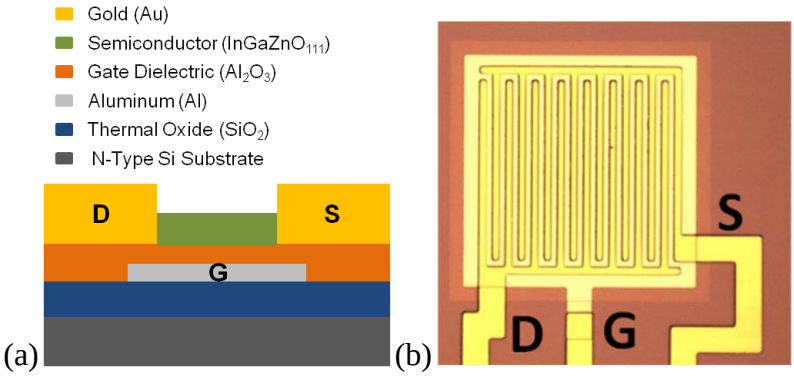


Figure 3.7: (a) Cross-sectional view and (b) micrograph of InGaZnO TFT.

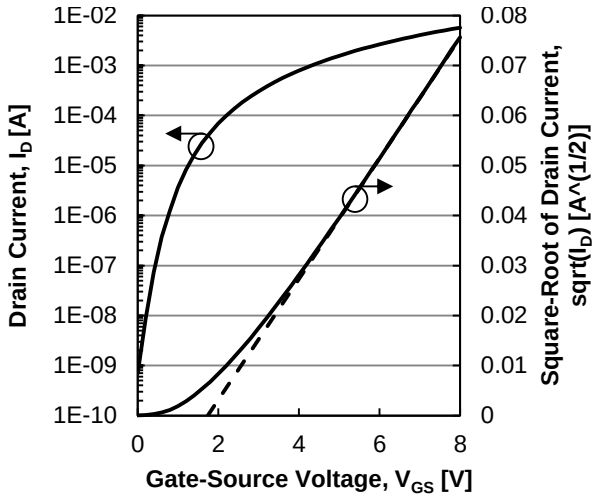


Figure 3.8: Transfer characteristic of TFT with 5µm channel length biased at 8V V_{DS}.

The gas measurements with InGaZnO TFTs were carried similar to the multi-functional impedimetric sensor measurement. Following each analyte exposure, a purge cycle was executed by flowing synthetic air composed of 20% O_2 and 80% N_2 over the device. Figure 3.11 depicts the response of a bare TFT biased in the saturation region with continuous DC biasing of $V_{GS} = V_{DS} = 8V$. The sensor shows a significant decay in I_{DS} during the windows of ethanol exposure, followed by an increase in current during the purge cycles. For example, 25500ppm of ethanol induced a downward ΔI_{DS} of 0.5-0.6µA or 5-6%.

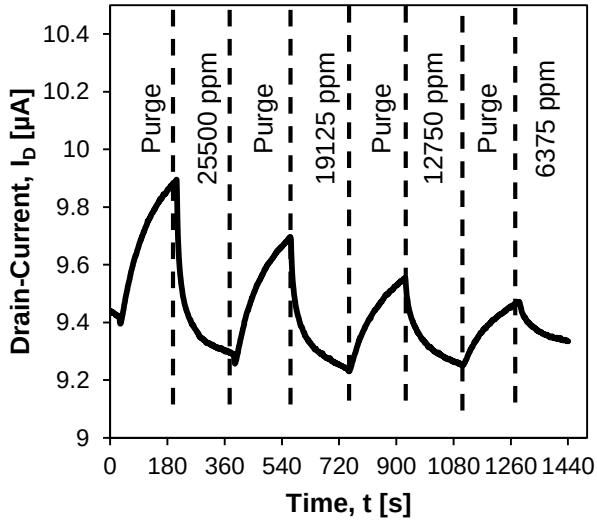


Figure 3.9: I_{DS} versus time upon different concentrations of ethanol exposure under constant V_{GS} and V_{DS} bias for a bare InGaZnO TFT.

A common technique for improving the sensitivity of VOC sensors involves the use of organic polymers capable of absorbing the analyte of interest. Again, PECH was used as it is known to absorb ethanol. Unlike the polymers that have been investigated in [111], which are conducting in nature, PECH is non-conducting. In this way, any fluctuation in I_{DS} must occur in the InGaZnO film itself. The response of the PECH-coated device, which was biased in the same manner as the bare device, is shown in Figure 3.10. Two main differences can be seen: (1) the polarity of the response has been inverted such that the presence of ethanol now causes a rise in I_{DS} and (2) the amplitude of the response has now increased. For 25500ppm, a ΔI_{DS} of approximately 2µA is recorded, which represents a 400% amplification of the response. However, the signal response appears more complex than in the case of a bare TFT.

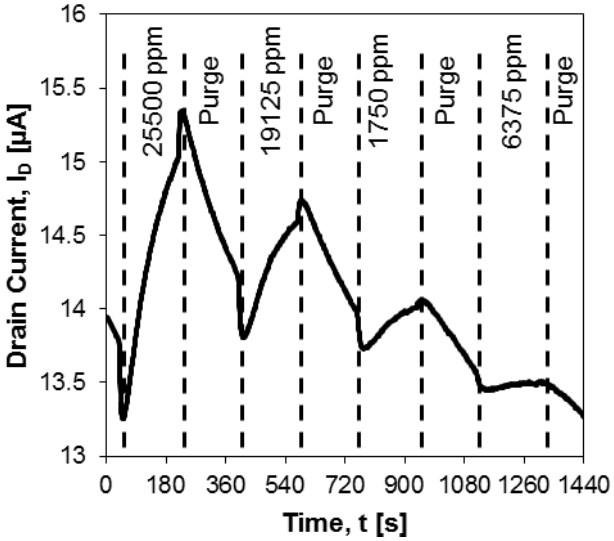


Figure 3.10: I_{DS} versus time upon different concentrations of ethanol exposure under constant V_{GS} and V_{DS} bias for a PECH-coated InGaZnO TFT.

It has been shown that a system-level strategy, namely duty-cycle operation, can be used to improve the device V_T stability in addition to the post-process annealing [112]. Hence, the response of a pulsed, bare TFT to different concentrations of ethanol while operating with duty cycle $\delta = 10\%$ was investigated. The result (Figure 3.11), though different to what was observed when continuous DC bias was applied, still shows changes in I_{DS}, which are proportional to the ethanol concentration. Interestingly, removal of the transient spikes between each cycle reveals a response that is, in fact, very similar to the PECH-coated TFT's response. Nonetheless, it is believed that the existence of these fast transients indicates the possibility of competing mechanisms, each with different time constants.

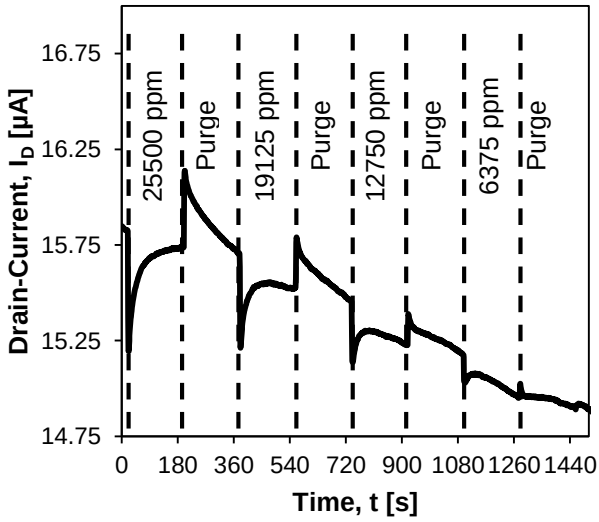


Figure 3.11: I_{DS} versus time upon different concentrations of ethanol exposure under pulsed V_{GS} and V_{DS} bias (δ = 10%) for a bare InGaZnO TFT.

CHAPTER 4

VERSATILE PASSIVE IMPEDIMETRIC SENSOR INTERFACE

A new interface circuit for passive impedimetric chemical sensors is described in this chapter. An overview of system architecture and operation principle will be given at the beginning of the chapter. Followed by the system overview, the specifications are reviewed and the state-of-the-art interfacing techniques summarized in Chapter 2 are revisited to explain the logic of establishing the proposed system architecture. Next, critical system blocks will be individually discussed and associated noise performances, which affect the system DR, will be analyzed. The goal of the noise analysis is not to derive comprehensive equations in terms of the component parameters (e.g., transistor size and AC parameters), but to gain insights in the noise behavior so that -relying on system and general design approaches- the overall noise level can be reduced. Based on the noise analysis, additional features such as chopper stabilization and oversampling will be incorporated in the full-system operation. At the end of the chapter, the full system performance, including linearity, noise performance, and SNR, is described.

4.1 System Overview and Operation

The core idea of the proposed system shown in Figure 4.1 is the convert the $R_{SEN}C_{SEN}$ product to a pulsewidth based on signal integration, using the so-called impedance-to-pulsewidth converter (ZPC). The integration is carried out by charging C_{SEN} and C_{INT} with a constant I_{REF_C}, while a constant I_{REF_R} is used to stimulate R_{SEN} (current stimulation). The fixed voltage across R_{SEN} and the ramping voltage across C_{SEN} are de-

noted V_{SEN_R} and V_{SEN_C}, respectively. The duration T_{RMP} needed to ramp V_{SEN_C} to the same voltage as V_{SEN_R} is proportional to the product of R_{SEN} and C_{SEN} + C_{INT}, described as,

$$T_{RMP} = \frac{I_{REF\_R}}{I_{REF\_C}} R_{SEN}(C_{SEN} + C_{INT}) \tag{4.1}$$

By fixing either C_{SEN} or R_{SEN}, a T_{RMP} proportional to resistance or capacitance values can be obtained. Assuming every block is ideal, a pulse with pulsewidth equaling to T_{RMP} can be generated after the EXOR logic by using two comparators to compare the upper and the lower potentials across R_{SEN}.

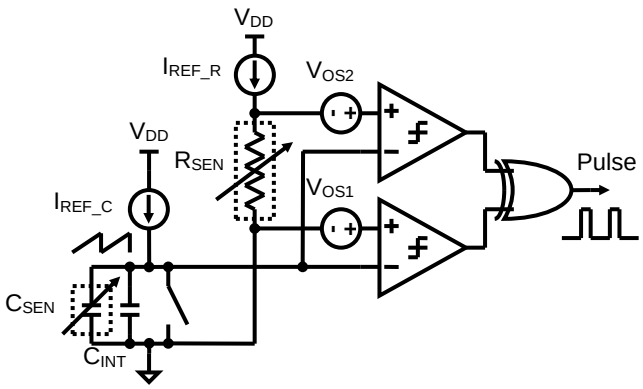


Figure 4.1: System level schematic of impedance to pulsewidth converter.

As the noise level is critical when measuring low R_{SEN} values, the capacitor C_{INT} is implemented on-chip to maintain good noise performance without using an external integration capacitor. In the capacitance measurement mode, C_{INT} only causes a pulsewidth offset T_{OFF} in T_{RMP} and T_{RMP} still increases linearly with the additional C_{SEN}.

One important and obvious circuit non-ideality is the input offsets of the continuous-time comparators. Ideally, the upper comparator should react after the lower compar-

ator. However, when V_{SEN_R} is smaller than the offsets or offset difference, making both comparator references close to ground (e.g., if I_{REF_R} = 10μA, R_{SEN} = 100Ω, then V_{SEN_R} = 1mV), different situations can happen depending on the amount and the polarity of offsets. For example, if both offsets are negative so that the comparators have references below ground, no pulse will appear at the output. The solution is to deliberately introduce offsets by unequally sizing the input differential pair of the comparators to meet the condition of $V_{OS2} > V_{OS1} > 0$. Thus, 20mV and 10mV offsets are added into V_{OS2} and V_{OS1}, respectively.

Another comparator non-ideality is the mismatch of the two comparator delays, T_{D1} and T_{D2}. Similar to the comparator offsets, if $|T_{D1} - T_{D2}|$ is greater than T_{RMP}, a faulty output can happen. However, the introduction of additional comparator offsets already solves this problem, as $|T_{D1} - T_{D2}|$ will be shown later to be much smaller than the T_{OFF} caused by $V_{OS2} - V_{OS1}$.

Finally, taking C_{INT}, comparator offset, and comparator delay into account, T_{RMP} in resistance T_{RMP_R} (4.2) and capacitance T_{RMP_C} (4.3) measurement modes can be expressed and rearranged as,

$$T_{RMP\_R} = (T_{D2} - T_{D1}) + \frac{C_{INT}}{I_{REF\_C}}(V_{OS2} - V_{OS1}) + \frac{C_{INT} I_{REF\_R}}{I_{REF\_C}} R_{SEN} \tag{4.2}$$

$$T_{RMP\_C} = (T_{D2} - T_{D1}) + k\frac{C_{INT}}{I_{REF\_C}} + k\frac{C_{SEN}}{I_{REF\_C}} \tag{4.3}$$

where k equals $V_{OS2} - V_{OS1} + I_{REF\_R}R_{SEN}$ and C_{SEN} is removed (C_{SEN} = 0) in the resistance measurement mode. The last terms in (4.2) and (4.3) represent the linear relations between resistance/capacitance and pulsewidth. The additional terms compose the pulsewidth offset T_{OFF}.

The next step is to define system level design parameters other than the intentional comparator offsets. The first one considered is the reference current I_{REF_R}. The critical resolution occurs at the resistance lower bound, which is 1Ω (1% of lowest target resistance of 100Ω). Assuming that a total $10\mu V_{RMS}$ noise level at the input of the comparators is attainable, the lowest possible I_{REF_R} is 10μA. Practically, the design should leave some margin and, thus, the target is to achieve better than $5\mu V_{RMS}$ noise level. Considering a maximum voltage of 0.5V below the circuit supply voltage, V_{DD} = 2.5V, the upper limit of R_{SEN} and the first sub-range to ensure proper operation of I_{REF_R} source can be determined, yielding a maximum of 200kΩ and a DR of 106dB. Similar to the margin concern in the lower bound, the upper bound of the resistance range is extended to 200MΩ and an I_{REF_R} of 10nA is found. Examining the lower limit of the upper sub-range, a 1kΩ (1% of 100kΩ) change approaches the noise level, which gives the required overlap (100kΩ to 200kΩ) between two sub-ranges.

To determine C_{INT} and I_{REF_C}, the digital resolution of V_{SEN_R} and ΔT_{RMP} has to be defined. V_{SEN_R} is defined to have 1μV digital resolution to avoid quantization errors to limit the circuit performance. While a fast ramping V_{SEN_C} requires a fine resolution in ΔT_{RMP}, a slow ramping V_{SEN_C} necessitates a very large C_{INT} and a tiny I_{REF_C}. A trade-off of 10ns per μV is chosen, corresponding to a 100V/s V_{SEN_C} ramp. Finally, C_{INT} and I_{REF_C} are set as 100pF and 10nA, respectively.

In terms of capacitance measurement, the critical resolution is 10fF when the baseline capacitance is 1pF. It should be noted that C_{INT} = 100pF should be included into the baseline to obtain the proper SNR and, thus, a SNR of 80dB must be achieved. The upper limit of measurable capacitance is bound by the 1Hz readout rate because an in-

creasing C_{SEN} reduces the slope of ramping V_{SEN_C}. However, the largest C_{SEN} of 1nF results in a 9.9V/s V_{SEN_C} ramp, which exceeds the supply voltage and is, thus, already reset within 1 second. Table 4.1 summarizes system level design parameters for the integrator, stimulation source, comparator, and digitization stage.

Table 4.1: Summary of system level design parameters.

Function or Block	Design Parameters
Resistance Stimulation	Noise $<5\mu V_{RMS}$ ($0.5\Omega_{RMS}$ or $0.5k\Omega_{RMS}$) Lower sub-range I_{REF_R} = 10μA Upper sub-range I_{REF_R} = 10nA
Integrator and Capacitance Readout	80dB SNR V_{SEN_C} = 100V/s I_{REF_C} = 10nA C_{INT} = 100pF
Comparator	Lower comparator V_{OS1} = 10mV Upper comparator V_{OS2} = 20mV Delay mismatch $\lvert T_{D1} - T_{D2} \rvert << 100\mu s$
Digitization	Resolution 1μV or 10ns

After the resistance is converted into a pulsewidth, the next step is the digitization. According to Table 4.1, the least significant bit (LSB) resolution is 10ns. Unless we have a clock faster than 100MHz, this time resolution cannot be achieved by only counting the clock. Even if the total 100μW power budget is devoted to the oscillator, generating a 100MHz $2.5V_{P-P}$ square wave is very challenging with a 0.35μm CMOS technology. One solution is to combine a coarse measurement with the system clock and a fine measurement close to the leading and the posterior edges of pulse with a time-to-digital (TDC) converter (Figure 4.2). The output digital code can be expressed as,

$$\text{Output Code} = N \times T_{CLK} + (k - m) \tag{4.4}$$

where N, T_{CLK}, k, and m are the number of clock cycles, one clock period in terms of

TDC code, the TDC code of leading edge, and the TDC code of posterior edge.

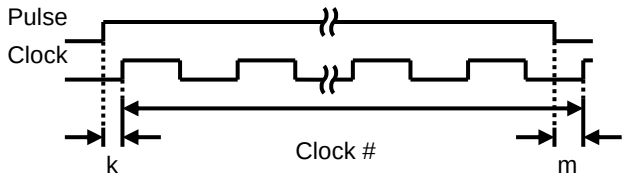


Figure 4.2: Operation principle of pulse width measurement technique.

4.2 Measurement Approach Considerations

While the core system has been presented in Chapter 4.1, the advantages of the proposed architecture compared to the state-of-the-art interfaces are discussed in the following. We begin this discussion considering the two major high-level resistance measurement approaches, namely V_{REF} stimulation (including RCOs) and I_{REF} stimulation, and revisit the associated system architectures summarized in Chapter 2. While considering the resistance mode, the ability for a specific architecture to perform capacitance measurements as well should always be considered.

The critical challenge of the passive impedimetric sensor interface is to achieve 160dB resistance DR at less than 100μW power consumption. Hence, the approach is to first satisfy this specification and then, with reasonable modifications, enable capacitance readout capability in the same system architecture. Before discussing and harnessing techniques introduced in Chapter 2, a more realistic chemoresistor model (compared to a simple resistor) is introduced in Figure 4.3. C_{par} and R_{par} are parasitic capacitance and resistance, respectively, which cannot be ignored in real designs [112]. C_{par} is in the range of few to tens of pF, depending on the sensor structure and sensing material; R_{par} ranges

from several Ω to 100Ω, and comprises contact resistances, metal line resistances, bonding wire resistances, and switch resistances. Corresponding V_{REF}-I_{SEN} and I_{REF}-V_{SEN} pairs with V_{REF} and I_{REF} stimulations in direct measurement configuration are depicted in Figure 4.3.

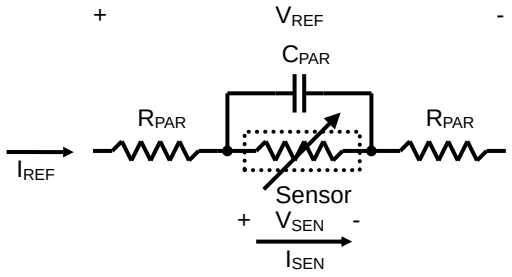


Figure 4.3: Simplified model of chemoresistor.

Using the direct measurement mode, V_{REF} stimulation results in a "fast" response in I_{SEN}, which is beneficial when discontinuous measurements are desired to reduce power consumption. The I_{SEN} response is considered fast because the transfer function of I_{SEN}/V_{REF} has a pole located at high frequency, $(2R_{PAR} // R_{SEN})\ C_{PAR}$, if V_{REF} is generated by an ideal voltage source. However, the V_{REF} stimulation results in a nonlinear I_{SEN}-R_{SEN} dependence, either intrinsically or extrinsically. In case of a large R_{SEN} ($R_{SEN} >> R_{PAR}$), such as for MOx sensors, I_{SEN} and R_{SEN} are inversely proportional with a constant product of V_{REF}. This intrinsic non-linearity can be corrected by calibrations or with the aid of a RCO by integrating I_{SEN} and measuring the oscillation period, which is proportional to R_{SEN}. In case of small R_{SEN}, such as for highly conductive polymer sensors, the extrinsic non-linearity caused by R_{PAR} can become prominent. To avoid the voltage drop across R_{PAR}, V_{REF} can be applied exactly across R_{SEN} through the high impedance nodes of a

regulation loop (Figure 4.4) composed of a differential difference amplifier and a pass transistor. However, the improvement in linearity sacrifices the speed of the V_{REF}-I_{SEN} response, which now depends on the bandwidth of the regulation loop. Even if the amplifier with the pass transistor has a wide bandwidth, the loop bandwidth is ultimately limited by $R_{SEN}C_{PAR}$. Besides the speed degradation, loop stability is a serious challenge. According to the specifications, the product of baseline resistance and parasitic capacitance changes by at least 140dB, which implies that the $R_{SEN}C_{PAR}$ pole could shift by more than 7 decades, making frequency compensation extremely difficult.

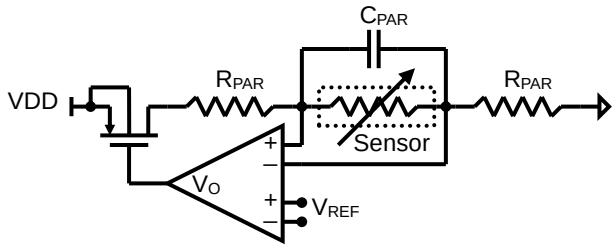


Figure 4.4: Regulated voltage mode direct measurement.

Most importantly, the lack of power control with V_{REF} stimulation is the crucial drawback in the desired low-power system. When V_{REF} is applied to the sensor, I_{SEN} increases dramatically with decreasing R_{SEN}. For example, V_{REF} = 100mV causes a 1mA current in a 100Ω resistor, the lower bound of the specified resistance range. Thus, to reduce power consumption, a very small V_{REF}, <10mV, would be required. Because on-chip voltage reference generators, such as bandgap references (BGR), generally exhibit high output impedance, V_{REF} should be buffered with a voltage follower. As the offset of the buffer could exceed V_{REF} due to process variations, auto-zeroing or chopping techniques are necessary, complicating the circuit design and operation. Furthermore, the additional

noise introduced by the buffer becomes a concern when V_{REF} is only several mV. By generating the small V_{REF} using a voltage divider, e.g., voltage summation BGR, or a small resistive load, e.g., current summation BGR, the noise from the original on-chip voltage generator can be scaled down, but the input noise of the final buffer that buffers the small V_{REF} does not benefit from this scaling effect. Hence, a small V_{REF} is normally noisy, causing degradation in the system SNR.

If V_{REF} stimulation is ruled out, RCOs, multi-functional interfaces, and impedance spectroscopy should be ruled out as well because they consistently process the I_{SEN} originated from V_{REF} stimulation. The potentially large I_{SEN} explains why RCOs and multi-functional interfaces usually consume power in mW range. Additionally, to achieve a wide DR, a high-speed comparator is required in the relaxation oscillator, normally the fundamental architecture of RCOs and multi-functional interfaces, to maintain oscillation at high frequency (or low resistance) range and minimize the non-linearity caused by the comparator delay. One should also note that the published RCOs and multi-functional interfaces usually do not include the necessary additional circuits, such as a counter, to provide a fully digital output. Both requirements ask for more power in addition to the sensor stimulation. Impedance spectroscopy appears to be able to achieve low power consumption, however, if careful examination is taken, those systems were characterized with small I_{SEN}, <100μA, implying that only high sensor impedances are applicable. At the same time, designing a low-output-impedance V_{REF} source to generate a clean sinusoidal wave on-chip is not an easy task. Consequently, for a low-power system, direct measurement with V_{REF} stimulation, RCO, multi-functional interfaces, and impedance spectroscopy are apparently not the best choices.

Considering the direct measurement in I_{REF} stimulation mode, the long response time is a drawback, especially when R_{SEN} and C_{PAR} are large. From Figure 4.1, V_{SEN}/I_{REF} has a pole at $R_{SEN}C_{PAR}$; however, this speed limitation may not be a serious issue in generally low-speed chemical sensing applications. On the other hand, I_{REF} stimulation exhibits two significant advantages. First, the measurement is intrinsically linear and enables a 4-wire measurement setup. Under a constant I_{REF} biasing, V_{SEN} is proportional to R_{SEN} and immune to R_{PAR} if V_{SEN} is sampled right across the sensor. Second, the power consumption is independent of R_{SEN} and only determined by the product of I_{REF} and supply voltage. Ideally, I_{REF} can be made as small as possible to reduce power; however, a small I_{REF} induces a small voltage change ΔV_{SEN} due to the resistance change ΔR_{SEN}, which may lie below the noise level at low baseline resistance. For instance, in order to detect a 1% resistance change, or maintain 1% linearity at 100Ω baseline (the lower bound of the specified resistance range) with a I_{REF} = 10μA, a noise level lower than 10μV needs to be achieved. On the other side, I_{REF} reaches an upper bound when V_{SEN} approaches the supply voltage; both bounds ultimately limit the DR of the whole system. To extend the DR, range division using different I_{REF} levels is a common approach [63]. Even though the 160dB specification can be easily achieved by combining multiple sub-ranges [52], the DR in each sub-range affects the number of required sub-ranges. Figure 4.5 illustrates that a 60dB sub-range DR requires six sub-ranges, while a 100dB sub-range DR requires only two sub-ranges to cover the full measurement range. Note that an overlap between adjacent sub-ranges is necessary to maintain sufficient linearity and SNR during transitions.

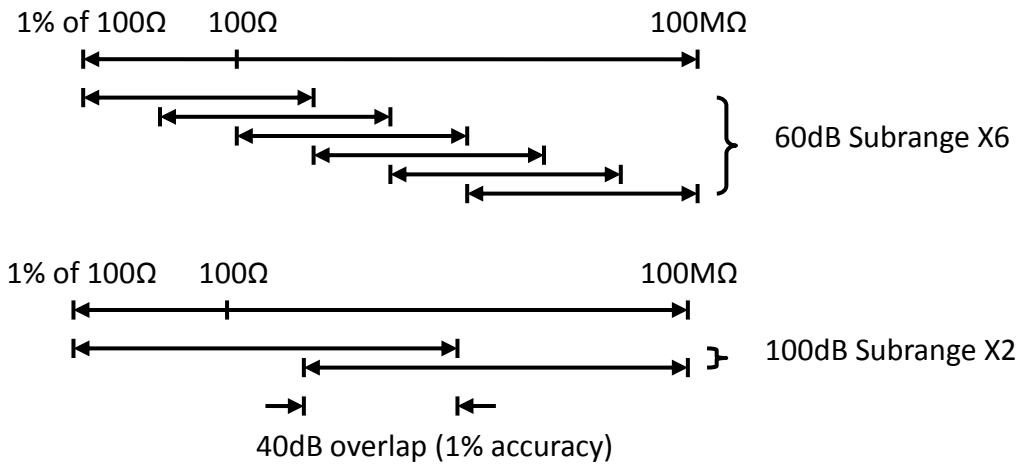


Figure 4.5: Relation between sub-range DR and sub-range number.

In practice, because of process variations, device mismatches, and non-idealities, sub-ranges are not lined up perfectly. Range offset and gain error [52] must be removed through calibrations; otherwise, poor full-range linearity could be the result. Being costly and time consuming, extensive calibration -usually performed post-fabrication- is what chip designers try to avoid. Unfortunately, realizing 160dB DR in one range is extremely difficult with low-power IC, and thus, maximizing the sub-range DR in order to minimize the sub-range number as well as the amount of calibration work is more reasonable. The 100dB sub-range DR (2 sub-ranges) shown in Figure 4.5 is practically achievable. During the simulation, the sub-range DR has to be more than 100dB to leave a margin for the gap after calibration, unexpected nonlinearity caused by leakage, and extra noise beyond device model, e.g., substrate, power supply, and connection lead noise. Despite the slow response and the DR challenges, I_{REF} stimulation is considered preferable in the present application in terms of power consumption and linearity. Next, the focus will be on realizing the given specifications using direct measurement in I_{REF} stimulation mode.

One way to achieve a low-power, high DR converter is to use a SC DSMs, which is the general approach for high-resolution ADCs. SC DSMs rely on over-sampling and a loop filter to push the quantization noise to a high frequency band, which requires a fast oversampling at the DSM input. In the ADC case, people assume the analog input to be an ideal voltage source so that the input voltage can settle down promptly after the beginning of the sampling phase. However, the $R_{SEN}C_{PAR}$ pole could reach a 1ms time constant in the extreme case and it takes at least 5 time constants to attain 1% accuracy. Moreover, the sampling capacitors of the DSM and parasitic capacitors (e.g., from layout and package) further increase the settling time. As long settling times usually occur when R_{SEN} and, thus, signal level are large and the low-noise requirement is relaxed, predetermining the R_{SEN} value to adequately reduce the oversampling rate may be a solution. But this method demands an extra predetermination ADC and complicates the control of the DSM and decimation filter. Besides the resistance measurement, we should also evaluate the possibility to enable capacitance measurement with the DSM architecture. In the literature, DSMs have been employed to perform capacitance measurements by replacing the sampling capacitors in the first integrator with C_{REF} and C_{SEN}. Considering the target specifications and employing a 1^{st} order, fully-differential DSM, the maximum 1nF C_{SEN} implies that at least two on-chip ~nF feedback capacitors are required in the first integrator to avoid saturation. Additional ~nF capacitors may be needed if a feedback architecture is chosen in a higher order delta-sigma loop. Considering the size of these capacitors, DSMs are not suitable for wide baseline capacitance range applications.

Since both R_{SEN} and C_{SEN} must be measurable parameters in the same system and RCOs output an oscillation period proportional to R_{SEN} or C_{SEN}, the RC integrator uti-

lized in RCOs (i.e., integrating I_{SEN} and periodically changing output state) is revisited and revised into an I_{REF} stimulation and non-oscillation architecture. Ultimately, by either fixing R or C, conjugate C_{SEN} or R_{SEN} can be measured.

4.3 Resistance/Capacitance to Pulsewidth Converter

The system diagram of resistance/capacitance to pulsewidth converter or ZPC is already shown in Figure 4.1. This sub-chapter details the transistor level implementation and, most importantly, noise behavior of each ZPC block. From Figure 4.1, four noise sources can be identified: the comparator, the integrator, the stimulation current source, and the reset switch. Assuming that all noise sources are uncorrelated, the total noise power is the summation of variance from the four noise sources. However, it should be noted that the pulsewidth is insensitive to the reset switch noise, because it only results in a common mode pulse shift at the beginning of the integration (Figure 4.6).

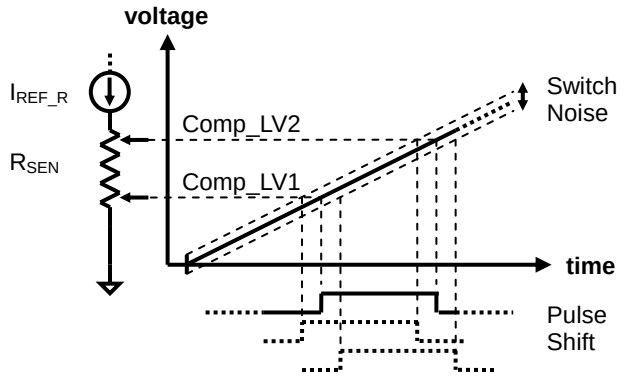


Figure 4.6: Illustration of pulse shift caused by switch noise.

4.3.1 Hysteresis Comparator

Continuous-time comparators with small hysteresis are used in the ZPC (see Figure 4.7). The particular concerns of comparator DC performance include input offset voltages, hysteresis windows, and delay mismatch. Monte Carlo simulations based on 100 samples show offsets of V_{OS1} = 11.46±1.31mV and V_{OS2} = 21.42±1.48mV, hysteresis windows of V_{HYS1} = 3.1±1.57mV and V_{HYS2} = 3.08±1.3mV, and delays of T_{D1} = 17.85±1.29μs and T_{D2} = 17.84±1.23μs. Noting the comparator offset locates at the upper edge of the hysteresis window and parameters with subscript 1 and 2 denote upper and lower comparators, respectively. Hence, the hysteresis windows always exist, V_{OS2} - V_{OS1} > 0, and the maximum delay mismatch (2.52μs) is much smaller than the minimum comparator offset induced T_{OFF} (71.7μs), guaranteeing T_{RMP_R} and T_{RMP_C} to be positive.

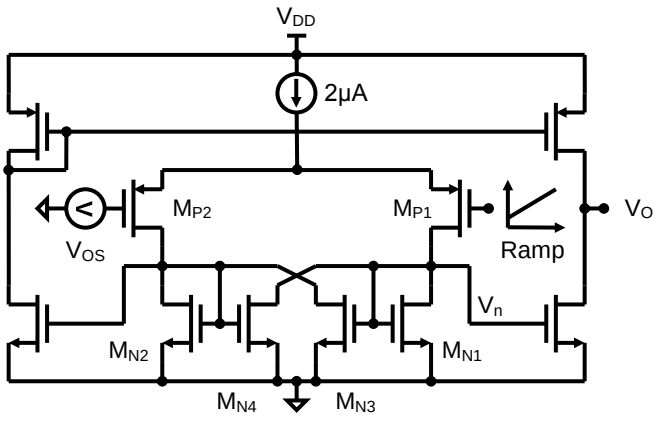


Figure 4.7: Schematic of hysteresis comparator.

Unlike for other continuous-time comparators, the conventional way of calculating noise by biasing the comparator at the transition point is not applicable for comparators employing positive feedback to generate hysteresis behavior. To introduce hysteresis,

the internal positive feedback (through M_{N3} and M_{N4}) should cause a net negative resistance and, thus, the gain and bandwidth cannot be calculated. Therefore, our approach is to observe the noise behavior right before the input ramping signal at M_{P1} gate reaches the transition point. The resulting small signal model of the differential stage is shown in Figure 4.8. It can be modeled as a bandwidth-limited gain stage followed by an ideal decision maker.

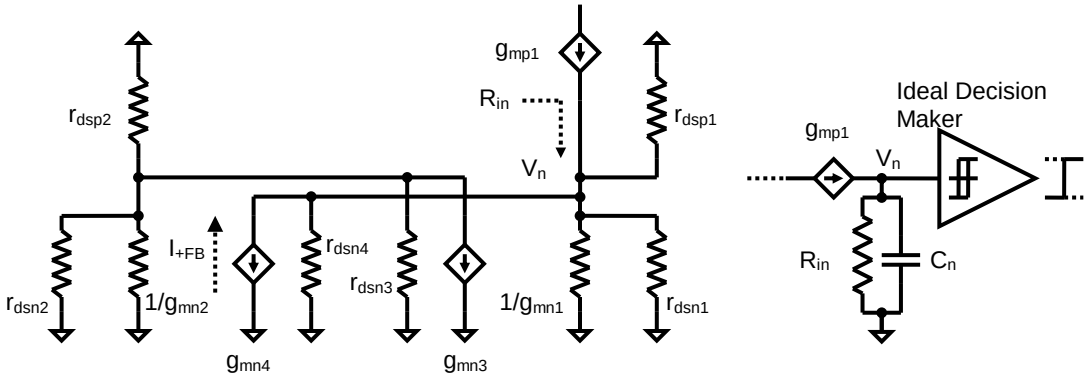


Figure 4.8: Small signal and simplified model of hysteresis comparator differential pair.

The decision to switch the circuit state is made when V_n is low enough (i.e., ramping signal at the gate of M_{P1} is close to the transition level) so that M_{N2} current, the portion of M_{P2} current beyond M_{N3} can drain, is sufficient to induce a net positive feedback. This happens when the net current flowing into R_{in} becomes zero, or in other words, R_{in} is infinite. With proper approximation, it can be found that the decision level can be expressed as a condition of for g_{mn2},

$$g_{mn2} \geq \frac{g_{dsn3}+g_{dsp2}}{k^2-1} \tag{4.5}$$

where $g_{dsn3} = 1/r_{dsn3}$, $g_{dsp2} = 1/r_{dsp2}$, and k is the ratio of width-to-length ratio (W/L) between M_{N3} and M_{N1} (M_{N4} and M_{N2} as well). It should be noted that g_{mn2} is smaller than

g_{dsn3} and g_{dsp2} as no current flows through M_{N2} initially. When the ramped input voltage (V_{SEN_C}) approaches the decision point, the positive feedback loop gradually wakes up. Since I_{+FB} flows against the incoming current induced by V_n, the equivalent R_{in} increases until V_{SEN_C} reaches the decision level. Hence, the bandwidth at the V_n node, determined by R_{in} and the total parasitic capacitance C_n, decreases. The increase in R_{in} also results in an increase in the DC gain, $g_{mn1}R_{in}$, and the noise level, $\overline{i_{n,tot}}R_{in}$, at the V_n node, where $\overline{i_{n,tot}}$ is the total RMS current noise at the V_n node. However, when the noise is referred back to the input of M_{P1}, the dependency of voltage noise level on R_{in} is removed. Thus, we can expect that the total input referred noise will decrease with the decreasing noise bandwidth at V_n. The simulation of gain and bandwidth of the differential pair as a functional of the voltage differential ΔV_{ID} from the decision level is shown in Figure 4.9.

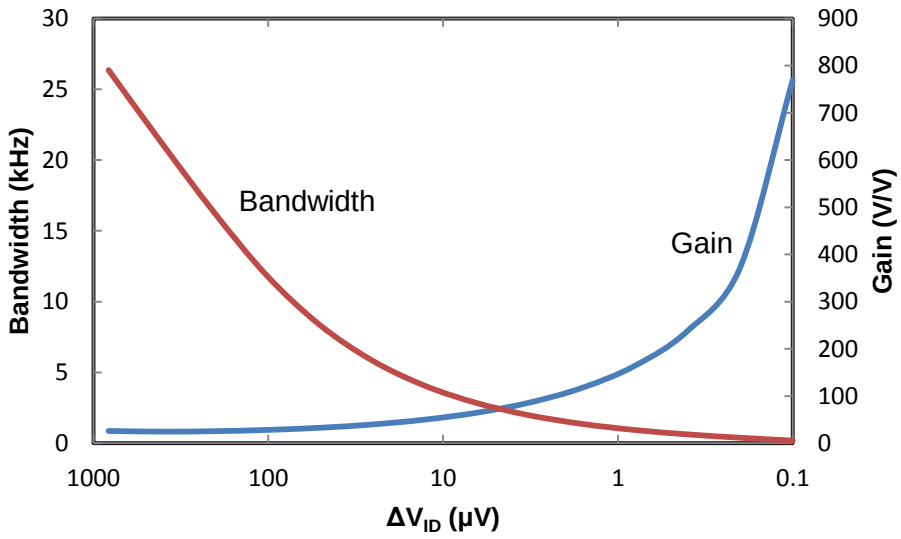


Figure 4.9: Simulation of gain and bandwidth of differential pair as a function of the voltage differential ΔV_{ID} from the decision level.

The simulation results for the gain and bandwidth are performed with an AC simulation by biasing V_{SEN_C} close to the decision level. Because V_{SEN_C} is within the hysteresis window, the DC operating point (OP) solutions may converge to either state. Choosing a proper algorithm and adequately adding convergence "helpers" such as current sources or conductances that do not affect circuit performance allow OP to converge to the desired state.

In Figure 4.10, the simulated total noise in the comparator is shown decrease with decreasing ΔV_{ID}. However, because the voltage differential ΔV_{ID} can effectively not become smaller than the RMS noise level of the inputs, the comparator noise remains finite. In other words, when ΔV_{ID} is close to the RMS noise value, the noise can trigger the positive feedback at any time. Assuming an RMS noise value of 5μV for ΔV_{ID}, the comparator input referred noise can is $5.63\mu V_{RMS}$ (Figure 4.10). Comparing to Figure 4.9, the bandwidth decreases about 10 times when ΔV_{ID} decreases from 1000μV to 5.63μV, while the noise power only drops by a factor of 3.5. While the thermal noise is reduced by N times if the bandwidth is N times narrower, the flicker (1/f) noise is only reduced by,

$$\frac{\mathrm{Log}_{10}f_{BW} - \mathrm{Log}_{10}f_{L}}{\mathrm{Log}_{10}(f_{BW}/N) - \mathrm{Log}_{10}f_{L}} \tag{4.6}$$

where f_{BW} is initial bandwidth and f_L is the lowest noise frequency of interest. It can be justified by separating thermal noise and 1/f noise to see their fraction with respect to the total noise as a function of ΔV_{ID}. Figure 4.10 shows that 1/f noise dominates the total noise power as ΔV_{ID} approaches the noise level.

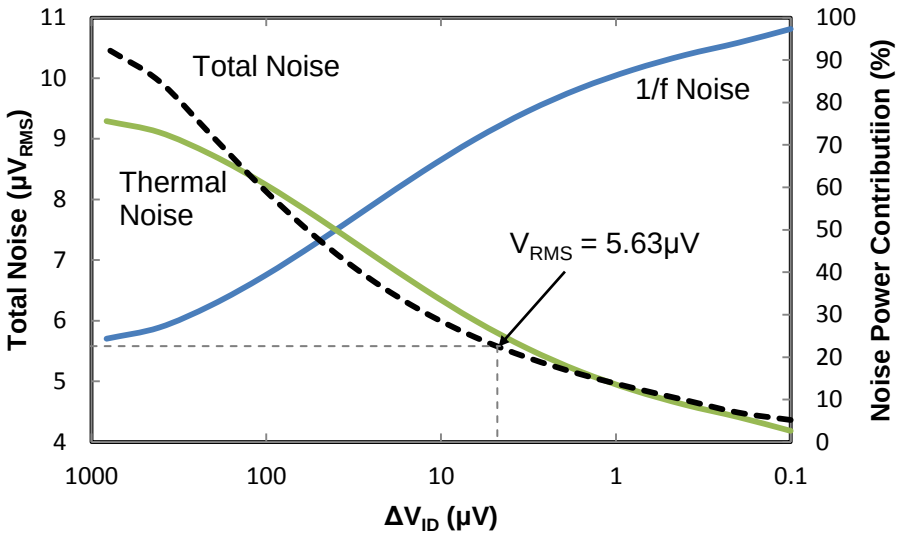


Figure 4.10: Simulation of comparator noise as a function of voltage differential ΔV_{ID} from the decision level. Dashed line is the total RMS noise and solid lines are percentages of thermal and flicker noise.

In fact, it is risky to rely only on the AC simulation result because the comparator is macroscopically a nonlinear circuit and biasing it extremely close to the sharp nonlinear transition edge could generate unreliable results even if the OP convergence deviates just slightly from the real OP. Hence, two additional simulations, periodic noise (PNOISE) and noise-enabled transient (TRAN), were performed to verify the AC simulation results. The periodic noise simulation is carried out by injecting a sawtooth wave at comparator input and measuring the phase noise of the output square wave. Then, the phase noise is converted into period jitter and, with known sawtooth wave slope (100V/s), referred back to the noise at the input. Figure 4.11 shows the phase noise simulation result. The RMS jitter is calculated to be 55.1ns, corresponding to a 5.51μV_{RMS} noise at the comparator input.

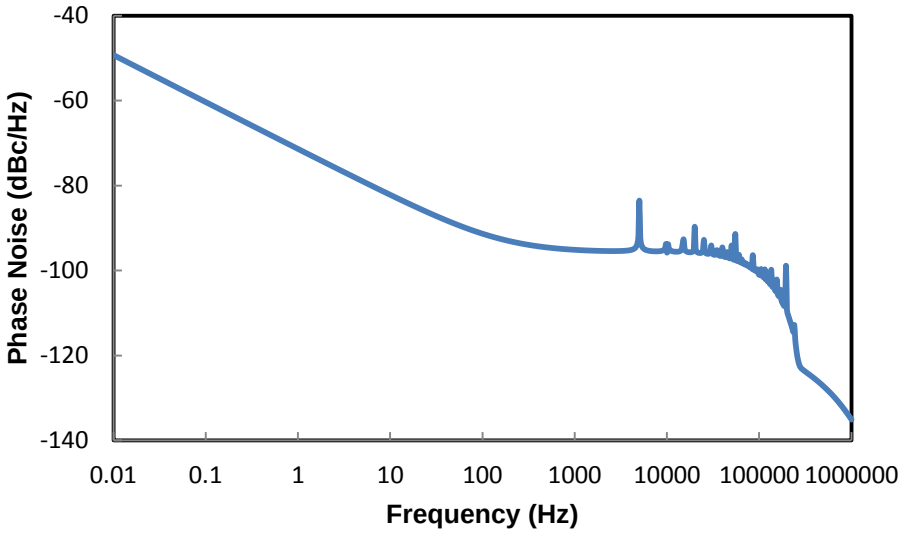


Figure 4.11: Phase noise simulation result at the output of comparator differential stage.

The noise-enabled transient simulation was carried out using the same schematic setup. However, a transient simulation with enabled transient-noise option was performed to acquire 500 cycles of jittering periodic waveform. Finally, period jitter and standard deviation functions were applied to obtain the RMS jitter of 113.4ns. The method that Cadence uses to calculate period jitter takes into account two noisy edges. If the two edges are subject to independent noise processes, the RMS jitter has to be divided by $\sqrt{2}$ (80.2ns); if they are subject to a fully correlated noise source, the RMS jitter has to be divided by 2 (56.7ns). Because the AC simulation shows that 1/f noise, which is considered highly correlated noise, dominates the total noise power around the decision level, the single edge noise lies between 56.7ns and 80.2ns and tends toward 56.7ns, corresponding to approx. 5.67μV_{RMS} input referred noise. The period jitter as a function of time is shown in Figure 4.12. In summary, AC, PNOISE, and TRAN simulations consistently show a noise level between 5 to 6μV_{RMS} for the comparator stage and, thus, the

simulation results are considered to be reliable.

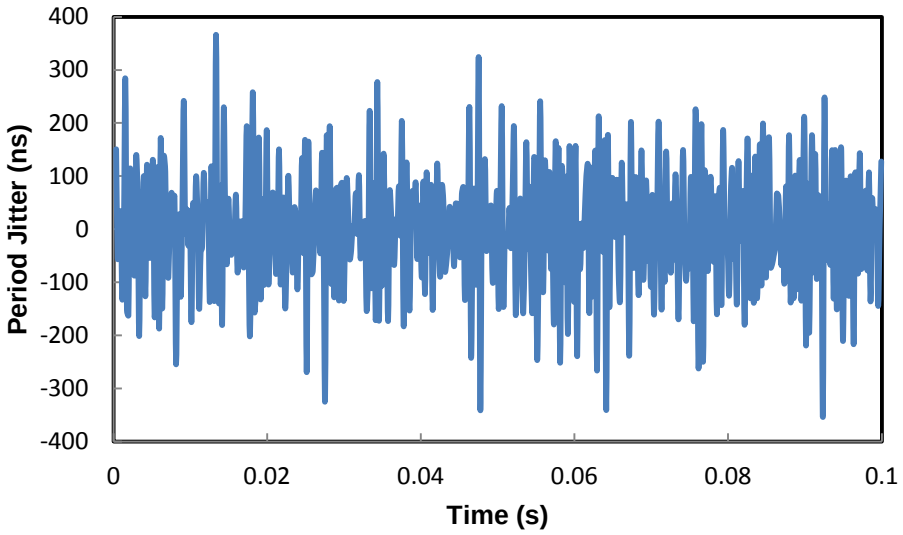


Figure 4.12: Period jitter simulation result at the output of comparator differential stage.

4.3.2 Integrator

The integrator comprises a 10nA current source mirrored from the primary on-chip current reference and a 100pF on-chip capacitor (Figure 4.13). Any voltage noise at the output of the integrator translates into noise in the switching times t_{C1} and t_{C2} and, thus, pulsewidth noise. The pulsewidth noise power is not simply the summation of variances at t_{C1} and t_{C2} points, because the noise at t_{C2} is partially correlated to the noise at t_{C1}. Suppose there is no noise gain between t_{C1} and t_{C2}, all noise at t_{C1} that causes a pulse shift will ultimately induces the same shift at t_{C2}. However, the noise gain between t_{C1} and t_{C2} may not be fully correlated to the t_{C1} noise, making t_{C2} noise partially correlated to t_{C1} noise. It is difficult to calculate the exact pulsewidth noise because the degree of correlation varies with pulsewidth (i.e., resistance value). However, because measuring the

pulsewidth, i.e., taking the difference between t_{C1} and t_{C2}, removes part of the t_{C2} noise that is correlated to the t_{C1} noise, an upper bound for the pulsewidth noise can be found by summing the variances in t_{C1} and t_{C2}.

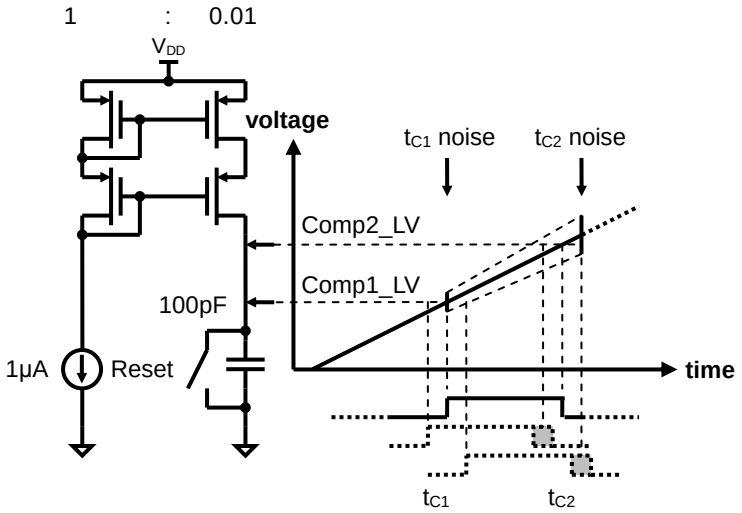


Figure 4.13: Schematic and integration waveform of integrator.

To analyze a periodically resettable integrator, a nonstationary noise analysis has to be performed. For white noise or thermal noise, this has already been done by injecting a wide-sense stationary (WSS) noise into a system at t = 0 (i.e., no noise when t < 0) [113]. The result for the integrated thermal noise power $\sigma^2_{\mathrm{Th.Int}}(t)$ is,

$$\sigma^2_{\mathrm{Th.Int}}(t) = \frac{1}{2} S_{x0} \int_0^t |h(\alpha)|^2 \, d\alpha \tag{4.6}$$

where S_{x0} is the one-sided thermal noise power spectrum density (PSD) and h(t) is the impulse response of the system. In the integrator case, h(t) is $u(t)/C_{INT}$ and u(t) is the unit step function. By replacing t with the integration time t_i, the result yields,

$$\left|\sigma^2_{\mathrm{Th.Int}}(t_i)\right| = \frac{S_{x0}}{2C_{\mathrm{INT}}{}^2}t_i \tag{4.7}$$

The thermal noise power is found to be proportional to t_i and, thus, the SNR of the integrator increases with $\sqrt{t_i}$ as the signal power is proportional to t_i^2. In other words, measuring a larger resistance (corresponding to a larger t_i) results in a higher system noise level, while the SNR still increases. In terms of capacitance measurement, it suggests that a large reference resistor leads to a better capacitance resolution.

However, the effect of 1/f noise has not been considered at this point. For 1/f noise, a similar approach to [113], where nonstationary thermal noise is analyzed in the time domain, is applicable. In the frequency domain, the integrated 1/f noise power is obtained by multiplying the 1/f noise PSD and the square of the frequency-domain transfer function, which varies with t_i. This multiplication in the frequency domain can be replaced with two convolutions in the time domain, resulting in,

$$\sigma^2_{1/f.\mathrm{Int}}(t) = R_{1/f.\mathrm{Int}}(t_1,t_2)\big|_{t_1=t_2=t} = h(t_1) * R_{1/f}(t_1,t_2) * h(t_2)\big|_{t_1=t_2=t} \tag{4.8}$$

where $t_2 > t_1 > 0$, and $R_{1/f.\mathrm{Int}}(t_1,t_2)$ and $R_{1/f}(t_1,t_2)$ are autocorrelation functions of integrated and original 1/f noise, respectively. According to the Wiener-Khinchin theorem, the autocorrelation function is the inverse Fourier transform of the two-sided PSD. Modeling 1/f noise as $S(f) \propto 1/f^{\alpha}$ and performing the inverse Fourier transform for the α = 1 case yields a constant $R_{1/f}(t_1,t_2)$,

$$R_{1/f}(t_1,t_2) = j\frac{S_{x0}\omega_c}{4} \tag{4.9}$$

where $\omega_C = 2\pi f_C$ is the 1/f noise corner frequency. Substituting the autocorrelation function in (4.8) with (4.9) and evaluating the convolution, the 1/f noise power can be found proportional to t_i^2 (4.10), which means SNR does not change with t_i when 1/f dominates

the total noise power.

$$\left|\sigma^2_{1/f.Int}(t_i)\right| = \frac{S_{x0}\omega_c}{4{C_{INT}}^2}{t_i}^2 \tag{4.10}$$

By equating (4.7) and (4.10), it can be found that 1/f noise will dominates the total noise power when

$$t_i > \frac{1}{\pi f_C} \tag{4.11}$$

The result of (4.10) and (4.11) are only approximations under the assumption that the full bandwidth of 1/f noise is considered. Thus, (4.9) is only valid when an infinite observation time is possible. An accurate result for the 1/f noise auto correlation function is derived by modeling 1/f noise as a result of white noise source driving an infinite long transmission line and performing a nonstationary noise analysis [114],

$$R_{1/f}(t_1, t_2) \propto \cosh^{-1}[\frac{1 + t_1/t_2}{1 - t_1/t_2}] \tag{4.12}$$

The 1/f noise PSD actually flattens at low frequency because of the finite observation time and thus the autocorrelation function is no longer a constant. Evaluating the two convolutions in (4.8) with (4.12) leads to a complicated equation. (4.12) shows that the 1/f noise at t_1 and t_2 are correlated, but that the correlation decreases as t_2 moves away from t_1. In the same publication, the analysis shows that the correlation decreases even faster if α deviates from 1. Comparing the extreme cases of thermal noise, i.e., no correlation between t_1 and t_2, and perfect 1/f noise, i.e., constant correlation between t_1 and t_2, it is reasonable to expect that the integrated 1/f noise will increase with $\sim {t_i}^{\beta}$ with $1 < \beta < 2$.

To verify the above analysis, a PNOISE simulation can be performed by resetting the integrator periodically. However, the spurs resulting from the periodic switching

could lead to an overestimation of the total RMS noise when evaluating the PSD integral across frequency range. This occurs when the number of point per decade of frequency is not large enough. If a large number of point is applied to the simulator, the simulation time will be unreasonably long. Although the noise-enabled TRAN simulation may be applicable, the time-consuming simulation would have to be performed multiple times with different t_i values. A better way is to employ a frequency domain analysis by mixing simulation and calculation. First, the original PSD of current source is simulated and extracted to be,

$$S_{REF\_C}(f) = \frac{5.49 \times 10^{-26}}{f^{1.109}} + 1.549 \times 10^{-27} \ (A^2/Hz) \tag{4.13}$$

Then, $S_{REF\_C}(f)$ is multiplied with the square of the time-limited integration transfer function $|H_{INT}(f, t_i)|^2$, which is also derived in [113] (see (4.14)), to obtain the integrated noise PSD $S_{INT}(f)$. The last step is to evaluate the integration of $S_{INT}(f) = S_{REF\_C}(f) \times |H_{INT}(f, t_i)|^2$ across the desired frequency range (1Hz to ∞ as the system is designed to have a 1Hz bandwidth) to find the total noise power. In this way, we simultaneously consider $\alpha \neq 1$ situation (i.e., using (4.13) as noise PSD), limited bandwidth (i.e., integrating from 1Hz), and a spur free spectrum (i.e., no switching noise).

$$|H_{INT}(f, t_i)|^2 = \frac{{t_i}^2}{{C_{INT}}^2} \mathrm{sinc}^2(\pi f t_i) \tag{4.14}$$

Figure 4.14 shows the power of total noise, thermal noise, and flicker noise as a function of t_i from 100μs to 20ms, corresponding to the minimum and the maximum integration time in one sub-range. Using a linear regression in the logarithmic plot, the integrated thermal noise and integrated 1/f noise are found to be proportional to t_i and $t_i^{1.83}$, respectively, which is consistent to the time-domain analysis. The integrated thermal

noise and integrated 1/f noise have a crossover point at t_i = 3.85ms.

To obtain the effective pulsewidth noise at the input of hysteresis comparator from the integrated noise shown in Figure 4.14, two additional modifications have to be applied. First, the filtering characteristic of the comparator with a pole around 2.5kHz must be considered. Hence, a low-pass transfer function $|H_{LPF}(f)|^2 = 1/(1+\omega^2/\omega_p^2)$, where $\omega_p = 2\pi\times 2500$rad/s, has to be included into $S_{INT}(f)$, resulting in $S_{INT}(f) = S_{REF\_C}(f)\times|H_{INT}(f, t_i)|^2\times|H_{LPF}(f)|^2$. Second, the upper bound for the pulsewidth noise is obtained by summation of the noise power at both t_{C1} and t_{C2}.

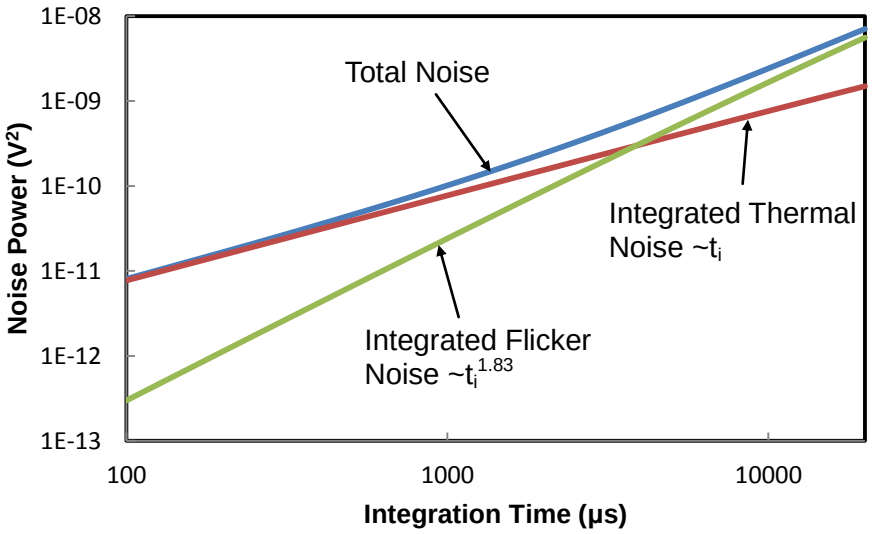


Figure 4.14: Simulated integrated noise components in the integrator as a function of the integration time.

The maximum effective RMS noise that causes pulsewidth variation and the SNR as a function of pulsewidth is shown in Figure 4.15. If only thermal noise exists, the SNR should increase at the speed of 10dB per decade. In the short pulse region, the SNR increase at 13.6dB per decade because the noise at t_{C1} is a constant; in the long pulse region,

SNR increase at 4.5dB per decade because 1/f begins to dominate the total noise power.

For resistance measurements, the RMS noise at the shortest pulsewidth ($4\mu V_{RMS}$) is important as it can be translated into the smallest resolvable resistance at the resistance lower bound. A $4\mu V_{RMS}$ noise corresponds to a $0.4\Omega_{RMS}$ noise at 100Ω. In terms of capacitance measurement, the maximum SNR is the major concern since a largest possible reference resistance can be chosen to maximize the SNR. To resolve 10fF capacitance with a 100pF offset (C_{INT}) at the capacitance lower bound (1pF) requires a SNR larger than 80dB. Figure 4.15 shows it can be obtained if the pulsewidth is larger than 1.2ms, noting that this does not include noise from other sources.

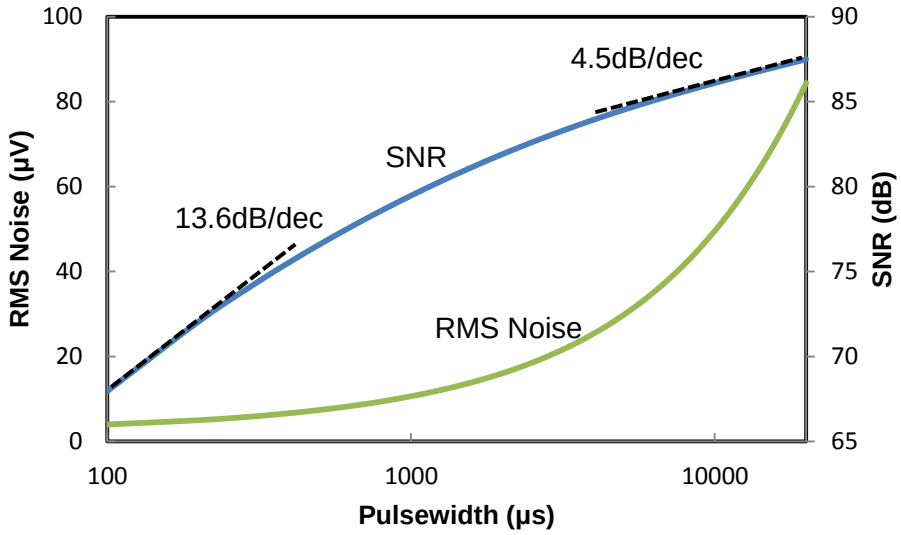


Figure 4.15: Pulsewidth SNR and RMS noise being referred to the input of hysteresis comparator (voltage noise) as a function pulsewidth.

4.3.3 Current Reference

The chemoresistor stimulation I_{REF_R} is generated using a current mirroring from the primary 1µA on-chip current reference. 1:10 and 1:0.01 current mirrors are used to

establish I_{REF_R} = 10μA and I_{REF_R} = 10nA for the low and high resistance sub-ranges, respectively. The 1:K_M cascade current mirror is shown in Figure 4.16. The major noise sources in the primary (left) branch are M_{P2} and M_{P4}, considering that the 1μA primary current source contains low-noise bipolar transistors, a ~kΩ resistor, and MOSFETs with source degeneration. Comparing M_{P2} and M_{P4}, the noise of M_{P4} is negligible due to the high source degeneration effect of M_{P2}. Thus, the noise PSD of the primary branch can be approximated by the noise of M_{P2} [115],

$$\overline{i_{n\_Pri}{}^2}(f) \cong \frac{8}{3}kTg_{m2} + \frac{K_f I_{D2}}{C_{OX}L_2{}^2}\frac{1}{f} \tag{4.15}$$

where k, T g_m, K_f, I_D, C_{OX}, and L, are Boltzmann constant, absolute temperature, transconductance, flicker noise coefficient, drain current, gate capacitance per unit area, and channel length of transistor M_{P2}. Then, the noise PSD contributed by the secondary (right) branch without R_{SEN} will be (in terms of M_{P2} parameters),

$$\overline{i_{n\_Sec}{}^2}(f) \cong K_M\left(\frac{8}{3}kTg_{m2} + \frac{K_f I_{D2}}{C_{OX}L_2{}^2}\frac{1}{f}\right) \tag{4.16}$$

if channel length of M_{P1} and M_{P2} are the same. The total reference current noise PSD is the sum of the mirrored primary branch noise and secondary branch noise. Given by,

$$\begin{aligned}\overline{i_{n\_REF}{}^2}(f) &\cong K_M{}^2\overline{i_{n\_Pri}{}^2}(f) + \overline{i_{n\_Sec}{}^2}(f) \\ &= \underbrace{K_M{}^2\left(\frac{8}{3}kTg_{m2} + \frac{K_f I_{D2}}{C_{OX}L_2{}^2}\frac{1}{f}\right)}_{K_M{}^2\times M_{P2}\text{Noise}} + \underbrace{K_M\left(\frac{8}{3}kTg_{m2} + \frac{K_f I_{D2}}{C_{OX}L_2{}^2}\frac{1}{f}\right)}_{M_{P1}\text{Noise}}\end{aligned} \tag{4.17}$$

If K_M > 1, the noise of I_{REF_R} is dominated by M_{P2}. On the other hand, if K_M < 1, , the noise of I_{REF_R} is dominated by M_{P1}.

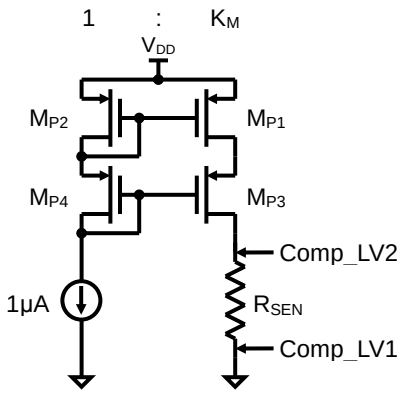


Figure 4.16: I_{REF_R} current mirror.

Now, considering the thermal noise contributed by R_{SEN} and the total current noise (4.17), the total voltage noise PSD across R_{SEN} can be estimated:

$$\overline{v_{n\_R}{}^2}(f) \cong 4kTR_{SEN} + \left(K_M{}^2 + K_M\right)\left(\frac{8}{3}kTg_{m2} + \frac{K_f I_{D2}}{C_{OX}L_2{}^2}\frac{1}{f}\right)R_{SEN}{}^2 \qquad (4.18)$$

(4.18) implies that the noise level is limited ultimately by the intrinsic R_{SEN} noise (first term) and that using long channel and small width-to-length ratio MOSFETs can minimize the additional noise contribution proportional to $R_{SEN}{}^2$ (second term). Because V_{SEN_R} is proportional to R_{SEN}, the resulting SNR across R_{SEN} increases at +10dB per decade increase in R_{SEN} if the intrinsic R_{SEN} noise dominates the total noise power; the SNR remains independent of R_{SEN} if the $R_{SEN}{}^2$ term dominates the total noise.

In the integrator sub-chapter 4.3.2, the analysis results suggested utilizing a large reference resistor for the capacitance readout mode to improve the pulse SNR, because the SNR increases with integration time. However, (4.18) implies that the pulse SNR could reach a ceiling at certain R_{SEN} values. Consequently, extremely long channel devices (L = 10-100μm) are used in the current source design to push the +10dB per decade SNR region towards large R_{SEN} values.

The simulation results for the RMS noise of the current references as well as the resulting SNR are shown in Figure 4.17. The low-pass filtering characteristic of the hysteresis comparator is also considered in the simulation. The performances of both the low and high resistance sub-ranges are plotted in the same graph. Clearly, SNR ceilings appear in both sub-ranges. In the low resistance range, the 10μA reference current is generated with K_M = 10, amplifying the R_{SEN}^2 term in (4.18) and, thus, the SNR reaches the ceiling (~82.8dB) earlier than for the high resistance range. It should be noted that this analysis does not include the noise contributions from the parasitic series resistance, nor the 1/f noise of the real chemoresistor. The former is generally negligible while the latter may strongly degrade SNR in real measurements.

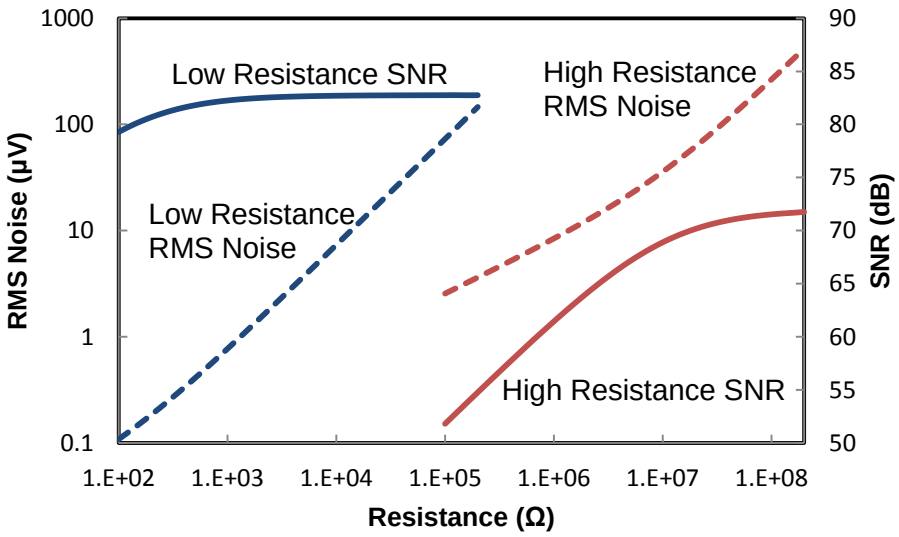


Figure 4.17: Simulation of RMS noise and SNR across stimulated chemoresistor.

4.3.4 Impedance to Pulsewidth Converter Behavior

So far, the individual circuit blocks of the impedance to pulsewidth converter (ZPC) have been introduced and their noise performance has been analyzed. In summary, the hysteresis comparator serves as a LPF and exhibits constant input referred noise while the noise of integrator and current reference are functions of t_i and R_{SEN}, respectively. Thereby, t_i and R_{SEN} are related to each other through the pulsewidth,

$$t_i = \underbrace{10^{-4}}_{\text{Comp1 Offset}}\ \text{sec.} + \underbrace{\left(10^{-4} + 10^{-2} I_{REF\_R} R_{SEN}\right)}_{\text{Pulsewidth (Comp2 Offset}-\text{Comp1 Offset}+\text{Resistance)}}\ \text{sec.} \tag{4.20}$$

(4.20) expresses t_i in two terms: the first term is induced by the offset (10mV) of lower comparator; the second term is essentially the pulsewidth induced by the difference of comparator offsets (10mV) and V_{SEN_R}. Ideally, the three noise sources are uncorrelated, and thus, the total noise σ_{ZPC}^2 is,

$$\sigma_{ZPC}^2 = \sigma_{Comp}^2 + \sigma_{Intg}^2 + \sigma_{Ref}^2 \tag{4.21}$$

Combing all simulation and calculation results, σ_{ZPC}^2 and the corresponding SNR are plotted in two separated graphs (Figure 4.18 and 4.19), one for the low resistance range and the other for the high resistance range. Thereby, the RMS voltage noise is converted into effective RMS resistance noise (Ω_{RMS}) and the SNR is the ratio of R_{SEN} and Ω_{RMS} in dB.

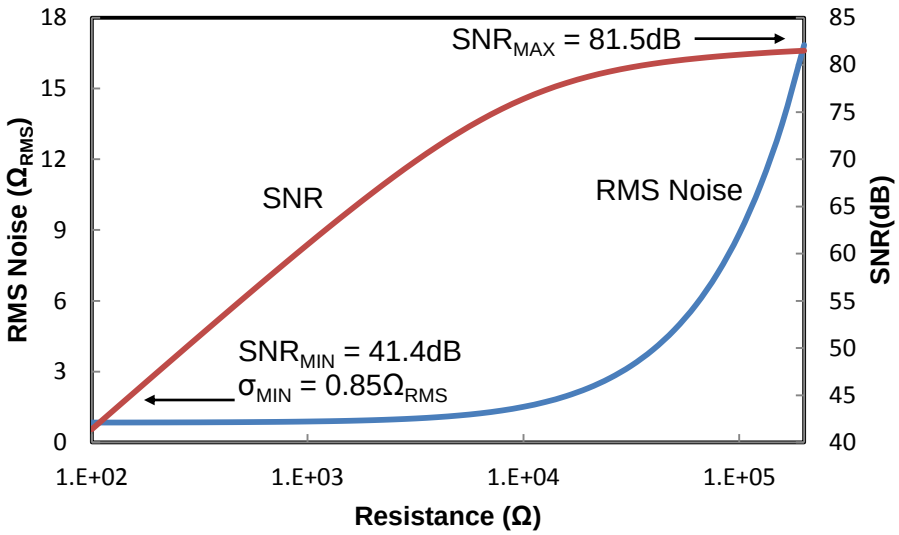


Figure 4.18: Total simulated RMS noise and SNR of the ZPC in low resistance mode.

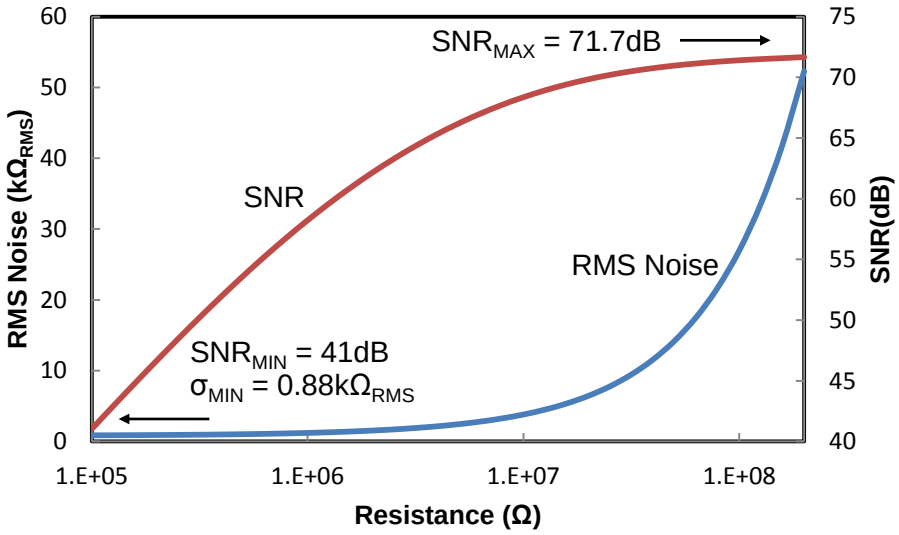


Figure 4.19: Total simulated RMS noise and SNR of the ZPC in high resistance mode.

For the resistance measurement, our focus is the minimum SNR spot, which is located at the minimum applicable readout resistance in each sub-range. In both sub-ranges, the minimum SNR requirement (40dB) is just obtained at the lowest re-

sistance, but they do not meet the tighter ZPC noise specification of 0.5 or 0.5kΩ_{RMS} (see Table 4.1). The performance might especially be not sufficient, because the noise of the digitization stage and unknown noise sources, such as the off-chip power supply, have not been included. For the capacitance measurement, the maximum SNR across the resistance range is the crucial performance metric since a maximum 80dB SNR is necessary to meet the maximum resolution requirement (10fF). Using a 200kΩ reference resistor in the low resistance range can reach 81.5dB SNR, but, similar to the resistance measurement case, it barely meets the requirement. Consequently, additional system level approaches have to be applied to further reduce the noise level.

Three noise reduction techniques, chopper stabilization, correlated double sampling (CDS), and oversampling, may be applicable in the system design. According to the noise analysis, the comparator noise (0.796Ω_{RMS}), which contains mostly 1/f noise, dominates the total noise at the minimum SNR spot (0.85Ω_{RMS}). Hence, applying chopper or CDS is more effective to remove 1/f noise. The chopper approach may not be applicable because of the idea to intentionally introduce offset voltages at the comparator input. For the maximum SNR point, about 75% of noise power is contributed by R_{SEN} and the reference current source. Chopper and oversampling/averaging approaches can be applied simultaneously to reduce both 1/f and thermal noise. Detail of the chosen approach will be described in section 4.5.

The measured total ZPC noise (solid line) is compared with simulation results (dashed line) in Figure 4.20 for both measurement sub-ranges. The measurement and simulation results follow a similar trend, but the measurement noise is approximately 50% larger than the simulated noise.

An Agilent MSO9404A high-performance oscilloscope was used to precisely record the pulsewidth variation. The on-chip comparators were buffered with a low-noise inverting stage and the pulsewidth, the time interval between two falling edges, was measured with the build-in function of scope. The integrator was externally reset with periodic pulses generated by a function generator and different chip resistors were manually connected to the measurement setup on PCB. A screen capture of an example measurement waveform is shown in Figure 4.21. Once 1000 samples were taken, the standard deviation of the time interval, i.e., the RMS noise of the pulsewidth, was recorded.

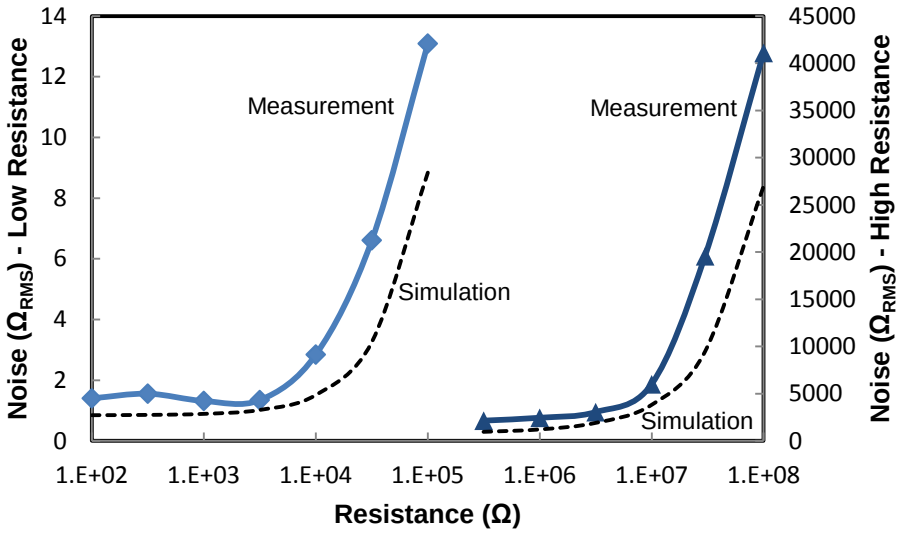


Figure 4.20: Measured (solid lines) and simulated (dashed lines) resistance noise of the ZPC as a function of the input resistance for the low-resistance (left axis) and high-resistance ranges (right axis).

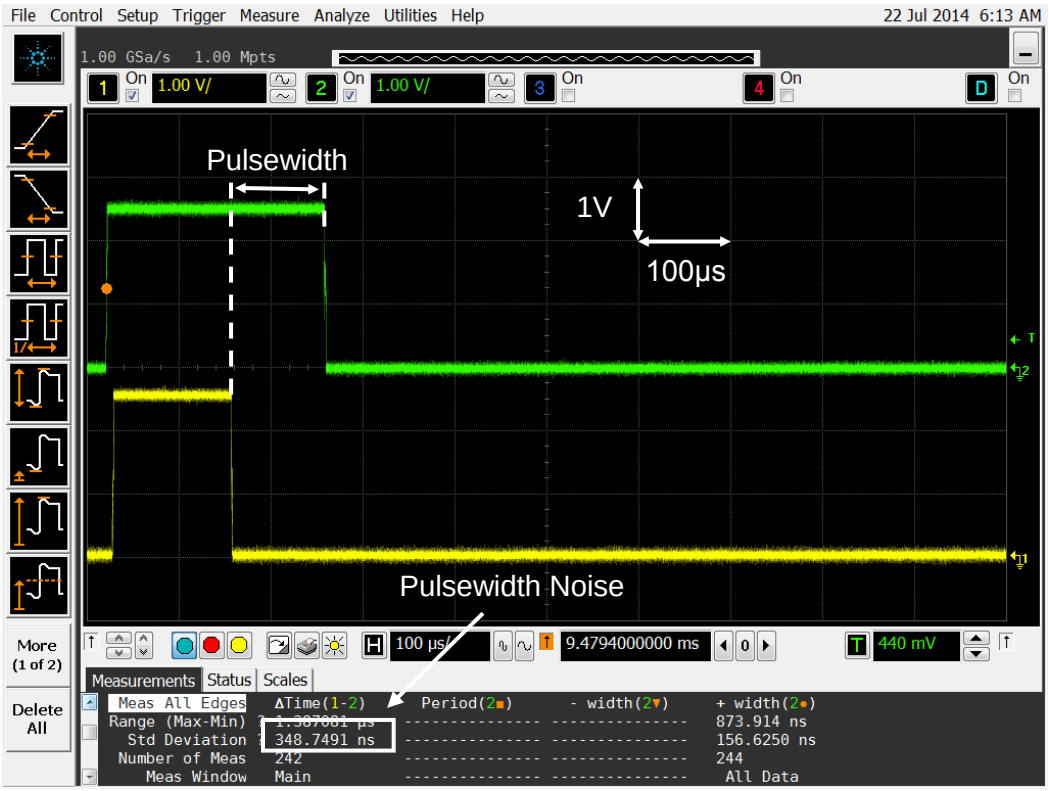


Figure 4.21: Measurement waveform for determining pulsewidth noise with 10Ω resistor. Upper and lower waveforms represent the output at the upper and the lower comparators, respectively. Because of inverting output buffers, negative instead of positive edges were observed at the transition points.

4.4 Pulsewidth Digitization

The detailed signal flow of the digitization with system clock and time-to-digital converter (TDC) is illustrated in Figure 4.22. The pulse output of the ZPC stage is fed into a clock counter and TDC to initiate and finalize the conversion process. The system clock is counted with the counter to perform the coarse conversion and fed into the TDC to determine an equivalent TDC code per clock period. Finally, using equation (4.4), the pulsewidth can be digitized with a resolution equal to the least significant bit (LSB) of the TDC.

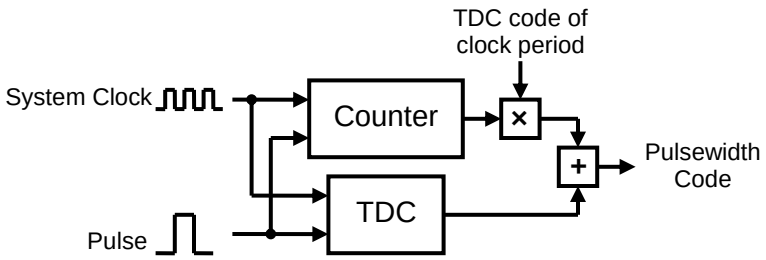


Figure 4.22: Signal flow diagram for digitization blocks.

4.4.1 Ring Oscillator

The system clock is generated by a current starving ring oscillator (Figure 4.23) consisting of 15 inverting stages. The individual stage delay is later used as LSB time reference of the TDC. This architecture exhibits two significant advantages: firstly, combining the system clock generator and TDC saves power; secondly, measuring the clock period with the TDC is no longer necessary because the period is always $2N_{STG}$ times the LSB, where N_{STG} is the number of delay stages in the ring oscillator. The current starving architecture is chosen to provide better control of the power consumption as the maximum current in each delay cell is limited by a current source. If a simple inverter is used as delay stage, the power consumption may vary significantly and exceed the power budget as a result of process variations. In addition, current sources are located between the drain terminals of NMOS and PMOS to obtain better signal symmetry [116], and each stage is buffered before feeding into the TDC logics and system control blocks.

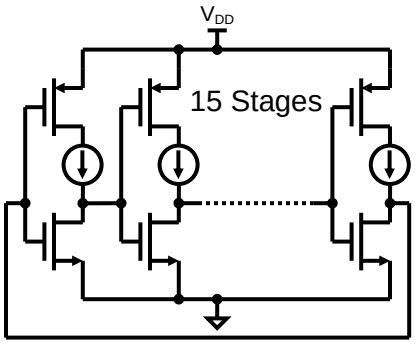


Figure 4.23: Current starving ring oscillator used as system clock source and TDC.

To achieve 10ns resolution (Table 4.1), the delay per stage is designed to be 5ns (LSB), corresponding to a 0.05Ω resolution. For a 15-stage ring oscillator, 5ns delay per stage is equivalent to a 6.67MHz clock frequency. Serving as the bridge between analog and digital signals, the clock signal generated by the ring oscillator affects the noise performance of the ZPC and is also sensitive to substrate noise from the digital blocks. Hence, the ring oscillator is placed in an independent isolation well with its own bias current source.

The ring oscillator introduces additional noise during the digitization, which is generally known as phase noise or clock jitter. Clock jitter is normally measured in two ways: using a precise counter or by measuring and integrating the phase noise with respect to the first harmonic. However, to find the amount of timing noise for different pulsewidths, it is incorrect to assume that each period jitter is uncorrelated and multiply period jitter by $\sqrt{N}$ to determine the N-period jitter [117]. Thus, counter and phase noise measurements are not applicable in the present application. Actually, the N-period jitter behaves similarly to the integrated noise, where the continuous integration becomes a discrete summation. When N is small, high-frequency uncorrelated noise is dominant and

the jitter is proportional to $\sqrt{N}$; when N is large, low-frequency correlated noise such as 1/f, power supply, and substrate noise comprises the major portion of jitter, causing jitter to be proportional to N. To determine the critical N where the noise behavior changes, cycle-to-cycle jitter measurements with different gate time have to be performed. The results are shown in Figure 4.24.

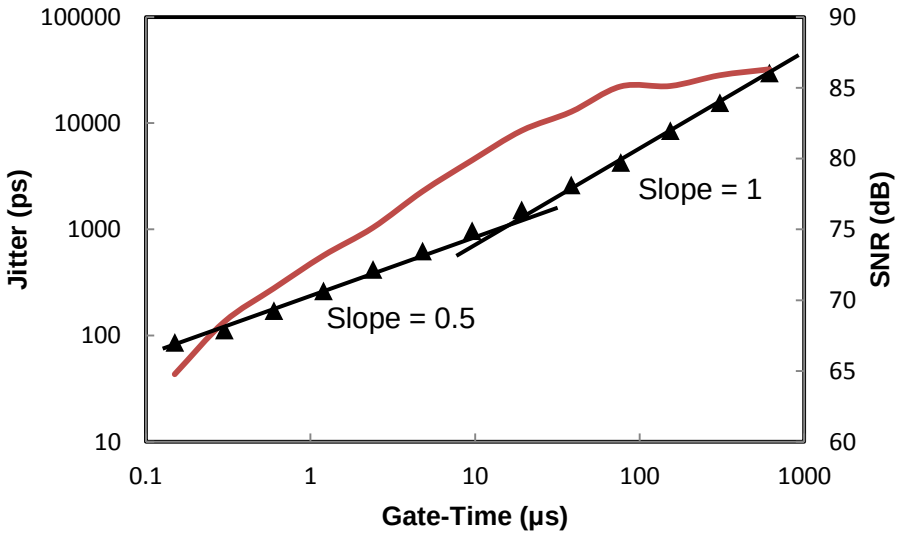


Figure 4.24: Measured cycle-to-cycle jitter and SNR of the ring oscillator as a function of the gate time.

Up to approx. 20µs, the jitter versus gate time plot has a slope of 0.5 when displayed in a logarithm scale. For gate times longer than 20µs, the slope becomes 1, as the correlated noise becomes the major noise contributor. The resulting SNR (Figure 4.24) tends to approach a constant value because of the correlated noise, indicating that the maximum attainable SNR is around 86dB.

Again, the measurement was carried out with the Agilent MSO9404A oscilloscope using a method similar to the one described in [117]. A power splitter separated the

oscillation signal into two identical parts: one feeds into the first channel of the scope and serves as the triggering signal, while the other feeds into the second channel and is delayed by the scope with the desired gate time. At the transition edge of the delayed signal, a histogram analysis was performed to obtain the time variation when crossing a fixed voltage level. A screen shot of the measurement waveform is shown in Figure 4.25.

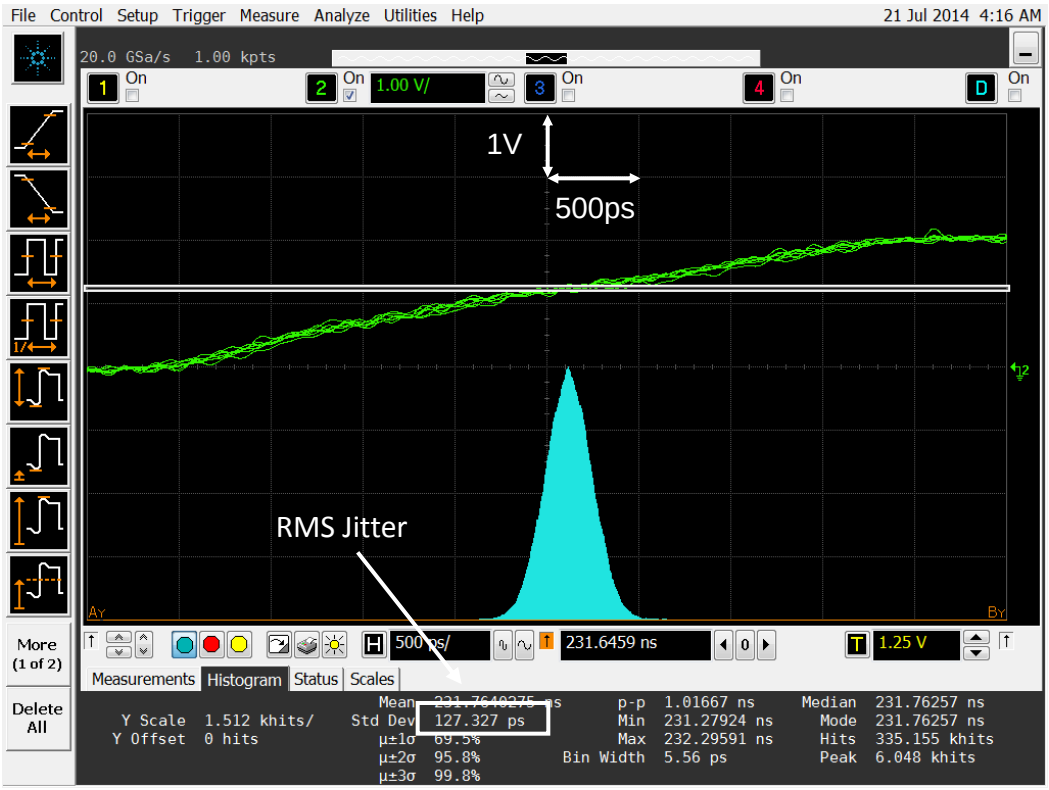


Figure 4.25: Measurement screen capture of cycle-to-cycle jitter. Jitter is measured by placing a decision level in the middle of clock transition edge and obtained a histogram of number of hits in time.

Using the measured noise data of the digitization stage and the ZPC, the total measured system noise (solid lines) and SNR (dashed lines) are plotted in Figure 4.26 under the assumption that ZPC and oscillator noises are uncorrelated. For gate times

longer than 614.4μs, the measurement data is extrapolated using the known noise trend. The resistance-equivalent noise level is shown on the left axis in units of Ω_{RMS} for the low-resistance range and in units of $k\Omega_{RMS}$ for high-resistance range. Clearly, the maximum SNR drops below 80dB and the minimum SNR is also below 40dB, which implies that system-level noise reduction is inevitable.

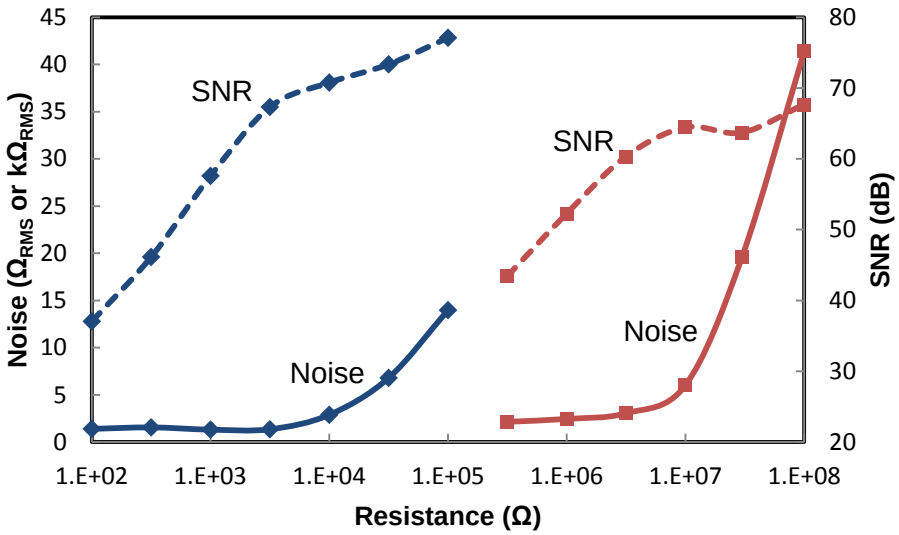


Figure 4.26: Measured total system noise of digitization stage and ZPC (solid lines) and corresponding SNR (dashed lines) as a function of the tested input resistance.

4.4.2 Time-to-Digital Converter

The block diagram and signal-flow of the full digitization stage is shown in Figure 4.27. The clock counter works closely with the TDC to perform the digitization and the analysis of TDC noise is not required since it is included in the ring oscillator noise (i.e., TDC is part of the ring oscillator). Essentially, this architecture is similar to a Vernier ring TDC [118], while the "ring" becomes a continuously running oscillator instead of a normally idle ring. Positive and negative edges of the input pulses serve as the

enable/disable signal to the counter, a TDC encoder, and an error bit correction block. The TDC encoder is a thermostat encoder performing,

$$\text{TDC Code} = \text{pop count}\left(a_{14} \oplus (a_0, \overline{a_1}, a_2, \overline{a_3} \ldots \ldots \overline{a_{13}})\right) + a_{14} \cdot 15 \quad (4.22)$$

to convert the ring oscillator output into a 5-bit binary code. When the encoder senses a pulse edge, the k (positive edge) and m (negative edge) values are determined by the TDC output at the rising/falling moments of edges and stored in the k and m register, respectively. The counter is enabled at the same time to count and register the number of coarse conversion clock cycles. In the cases when the encoder outputs a maximum code, a miscount or an over-count could have happened. Hence, the error bit correction block accounts for this situation.

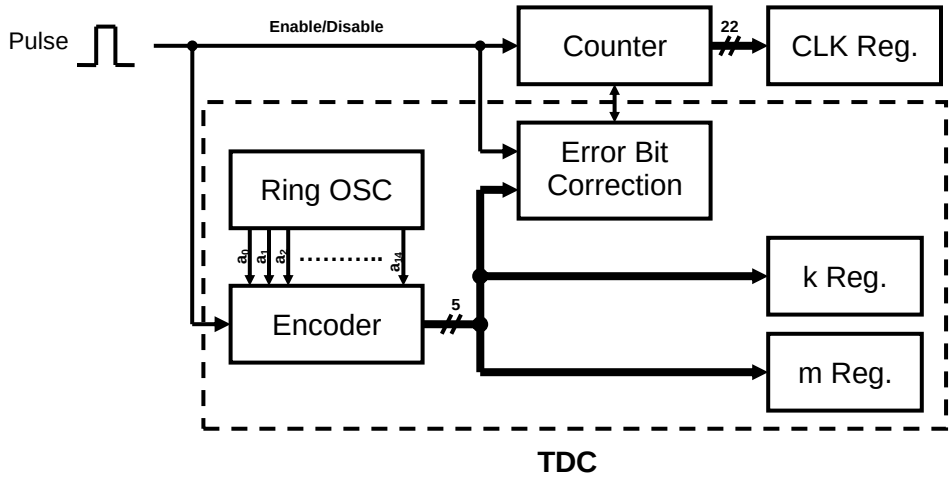


Figure 4.27: Signal flows and block diagram of the digitization stage.

Figure 4.28 illustrates the error count situation in the digital signal timing diagram. When the edge of pulse appears close to the end of the maximum TDC code, the TDC should still be recorded as 29 and one count in the counter should appear immediately

right at the transition of TDC code. However, if a delay causes the counter being enabled after the TDC code transition, a miscount will happen. In the same manner, an over-count will happen at the negative edge.

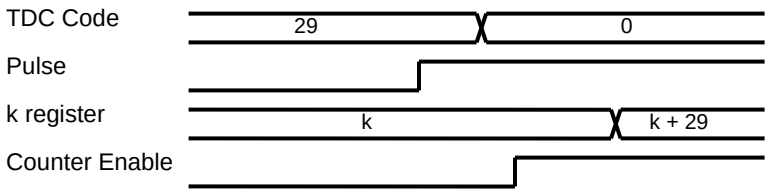


Figure 4.28: Digital timing diagram of an error count occurrence example.

A hardware-based finite state machine (FSM) that performs the correction algorithm is shown in Figure 4.29. As a pulse edge is detected and the TDC output code is 29, the error bit corrector begins a follow-up process. If the pulse edge is positive and no count appears in the counter within 10ns, the counter will be forced to up-count once. On the other hand, if the pulse edge is negative but a count happens within 10ns, the counter will be forced to down-count once.

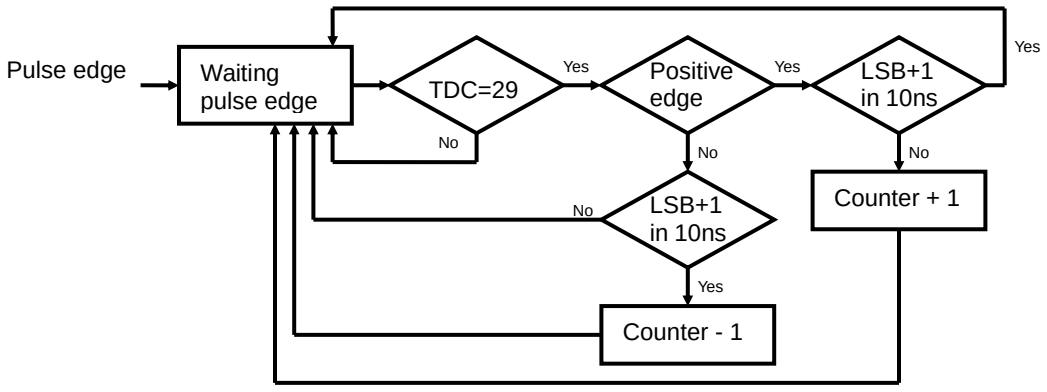


Figure 4.29: Algorithmic state machine (ASM) diagram of error bit correction function.

4.5 Full-System Operation

The measured resistance noise in Figure 4.26 exceeds the specified noise levels. Hence, we apply chopper, CDS, and oversampling techniques by modifying the primitive ZPC-digitization architecture and performing suitable operations. The modified system diagram including the noise suppression techniques is shown in Figure 4.30.

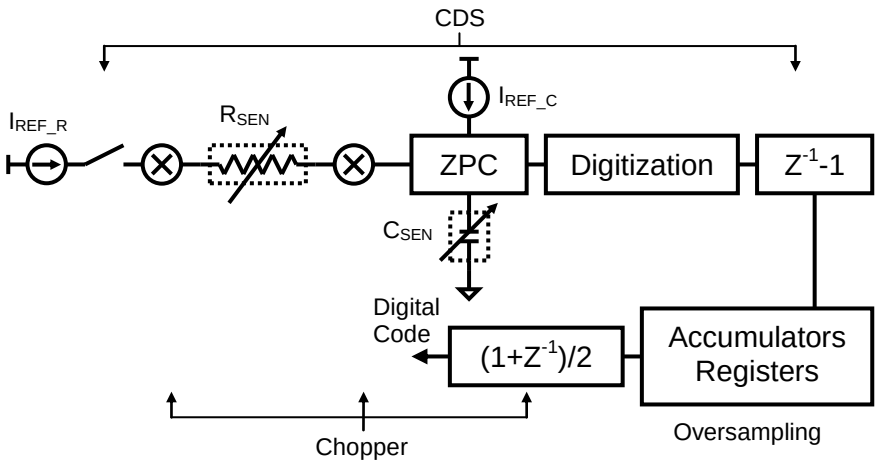


Figure 4.30: Full system diagram and associated noise suppression techniques.

All system blocks are implemented on-chip, except for the $(1+Z^{-1})/2$ function, a part of the chopper, and an averaging function after oversampling. The control digital block is implemented with a FSM. A chopper is applied across the chemoresistor to avoid R_{SEN} 1/f noise and, at the same time, realize a pseudo-AC stimulation to mitigate polarization effects. The applied chopper is slow as it follows the system readout rate (1Hz). CDS is accomplished with a switch and a Z^{-1}-1 function by a digital subtractor. In the first readout, I_{REF_R} stimulates R_{SEN} and, thus, the ZPC generates a pulse duration associated with V_{SEN_R} and the comparator offsets. In the second readout, I_{REF_R} is turned off and only the comparator's offset information is left in the pulse. The subtraction between

two consecutive readouts yields a pulsewidth that is a linear function of R_{SEN}. Hence, the CDS is effective to remove the 1/f noise of comparators, which is the major noise contributor in the low SNR region. The CDS frequency is variable, depending on R_{SEN} value. Lastly, the oversampling is simply done by taking measurement multiple times and averaging at the end of each measurement cycle. Measurement results with system-level noise suppression will be discussed in Section 4.6.

Within the one-second readout period, as many measurements as possible are taken until about 0.7 seconds. The remaining 0.3 seconds is reserved for finishing the last readout and for exporting data. When R_{SEN} is small, each integration interval is short, leading to a high OSR and fast CDS. For large R_{SEN}, the OSR is reduced automatically to allow more time for the input signal to settle down. In fact, the input settling and the integration share the same time interval. OSR lies in the range from 30-3500 and, thus, the CDS frequency is from 30Hz-3.5kHz. Digitized pulsewidth and measurement counts (OSR) are continuously accumulated in several registers. Finally, the raw data containing k, m, clock, and OSR values are transmitted through a serial bus.

As the name suggests, the proposed system is reconfigurable for different measurement purposes. Table 4.2 displays and highlights all feasible measurement modes with checked boxes. For the differential resistance measurement, the CDS is performed implicitly by the subtraction of reference pulses which contain both information of the comparator offsets and the reference resistance.

Table 4.2: Possible measurement mode of interface circuit.

		Single-ended	Differential	Pseudo-AC
Resistance Measurement	100-200kΩ	X	X	X
	100k-200MΩ	X	X	X
Capacitance Measurement		X		

4.6 Full-System Characterization

The interface system is fabricated with a 0.35μm BiCMOS process. A microscopic die picture is shown in Figure 4.31. The interface circuit occupies 1.7mm×1mm, excluding pad area, with the ZPC and digitization stage separately shown in the picture.

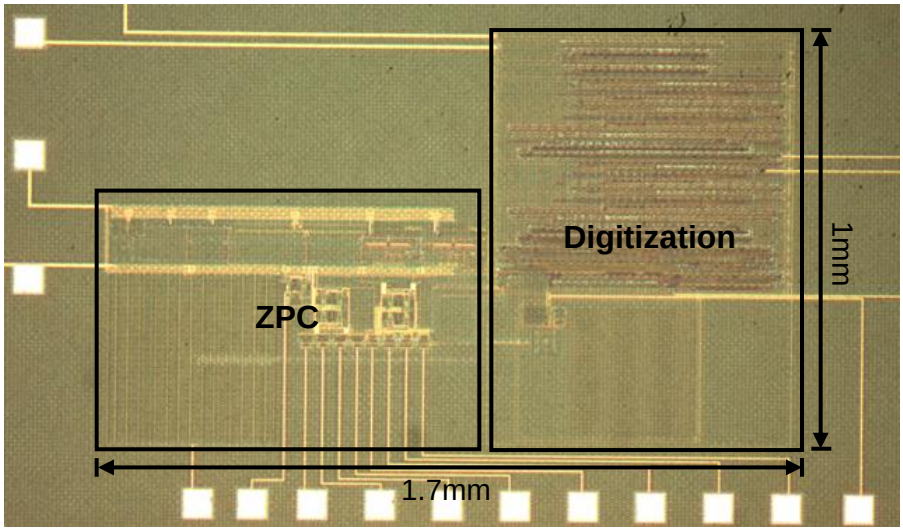


Figure 4.31: Microscope image of the chip containing the impedimetric chemical sensor interface, fabricated in 0.35μm Texas Instrument BiCMOS process. The circuit occupies an area of 1.7mm×1mm.

For the characterization, the interface chip was mounted and wire-bonded to a 44-pin leaded chip carrier (44LDCC), which was attached to a measurement PCB (See Appendix). The PCB provides a 2.5V supply voltage, pads for soldering test resistors and

capacitors, switches to select the operation modes, and buffers for communicating with a computer. Test resistors from 10Ω to 200MΩ and test capacitors from 0.1pF to 1nF with 10 logarithmically spaced values per decade were manually soldered to the PCB and tested. Commercial chip resistors and capacitors with best accuracy and temperature coefficient were purchased. A wait-time of 15 minutes between each measurement allowed PCB and components to cool down after soldering. The serial data readout was synchronized and recorded with LabView through a DAQ card. Since a complete measurement took more than a week, the interface chip and measurement PCB was placed in an environmental chamber at 22℃.

Figure 4.31 and Figure 4.32 compares the measured noise level and resulting SNR before and after applying the system-level noise suppression techniques. The noise was obtained by analyzing the output digital values acquired over 5 minutes. The dashed curves represent the measured jitter noise from Figure 4.26. Blue and grey curves are noise-suppressed results in single-ended and differential resistance measurement modes, respectively. The missing SNR in differential mode is due to the unavailable signal level, which is simply the resistance value in the single-ended mode. The differential measurement was carried out with two resistors having normally the same resistance values. The applied techniques are shown to be effective in noise suppression. The improvement of SNR is about 15dB for the low-resistance mode and 20dB for the high-resistance mode, corresponding to 32 and 100 times reduction in noise power, respectively. The SNR is now >51dB from 100Ω to 100MΩ and the maximum SNR is 87.6dB. For long integration times (i.e., close to 100kΩ and 100MΩ in low and high resistance modes, respectively), the differential-mode operation shows lower noise levels compared to the sin-

gle-ended mode, because the CDS cannot efficiently remove the integration noise of the integrator and the digitization stage when the measurement phase has an integration period much longer than the CDS phase. The maximum SNR is also limited by this integration noise.

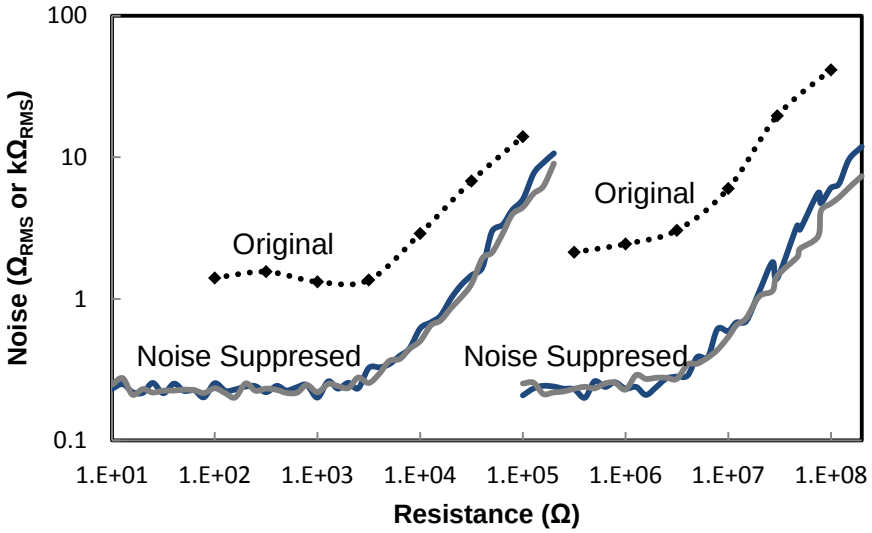


Figure 4.32: Comparison of measured system noise level (expressed as noise-equivalent resistance change) as a function of test resistance before and after applying noise suppression techniques.

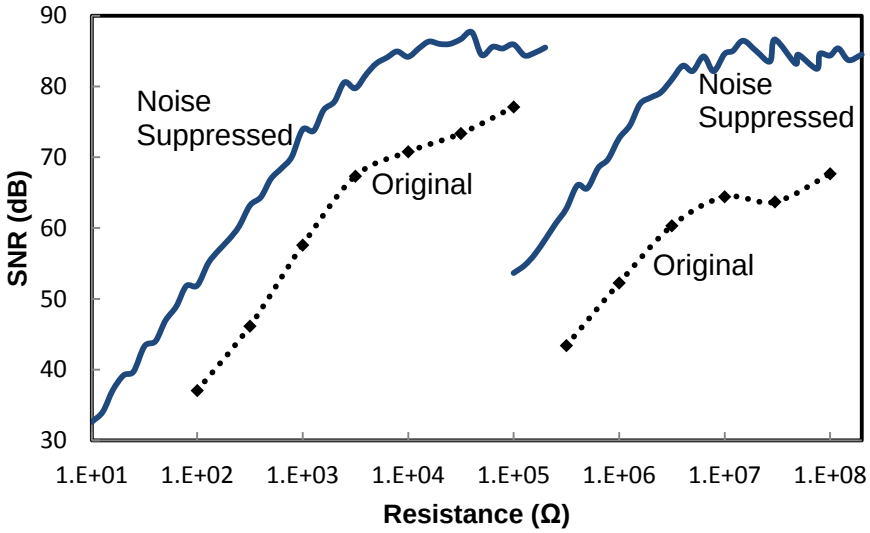


Figure 4.33: Comparison of extracted SNR as a function of test resistance before and after applying noise suppression techniques.

The noise performance of the capacitance measurement mode is measured in the same manner with 10 capacitance values per decade from 0.1pF to 1nF. A 100kΩ reference resistor is used for the measurement. Measured noise levels expressed as noise-equivalent capacitance fF_{RMS} and the associated SNR values are shown in Figure 4.33. When calculating SNR, the offset (108.982pF) including the on-chip integration capacitor and all parasitic capacitances have been removed. The interface achieves >40dB SNR at minimum of 0.8pF C_{SEN}.

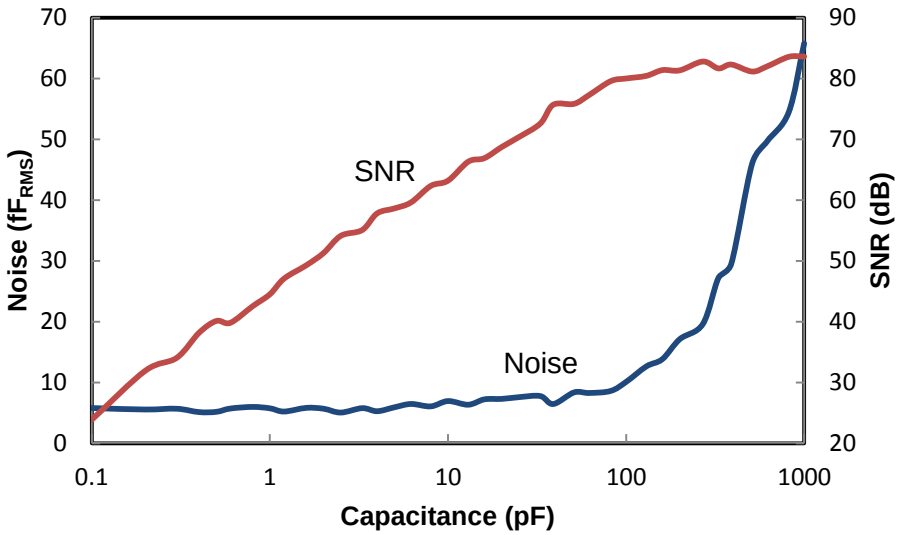


Figure 4.34: Measured noise level expressed as noise-equivalent capacitance and resulting SNR as a function of test capacitance in capacitance measurement mode.

Besides the noise measurement, an even more important system characteristic is the system linearity. Linearity and noise were actually measured simultaneously. The linearity is calculated from the average value of recorded data, while the noise is extracted from the standard deviation. For the noise measurement, the precision of the tested resistance and capacitance values is not a major concern, whereas it is vitally important when investigating the system linearity. Hence, the resistance of the test resistors was measured with an Agilent 34401A high-precision multi-meter and the capacitance of the test capacitors was measured with an Agilent 4284A precision LCR meter. The linearity measurement results for resistors and capacitors are shown in Figures 4.34 and 4.35, respectively.

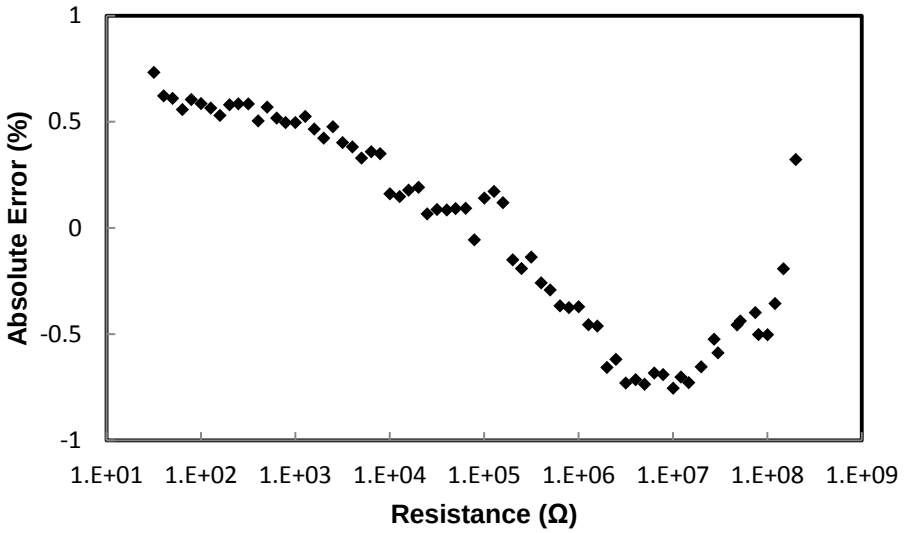


Figure 4.35: Measured system linearity in resistance measurement mode linearity from 31.6Ω to 200MΩ.

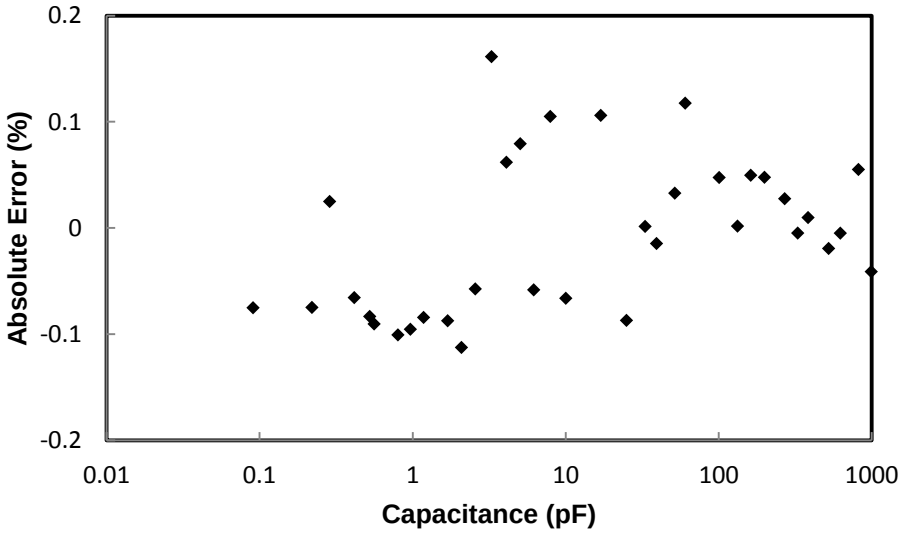


Figure 4.36: Measured system linearity in capacitance measurement mode from 0.1pF to 1nF.

The resistance linearity is measured and calculated after calibration. Since the whole resistance range is covered by two sub-ranges, which is the major advantage of the

proposed interface, only a single calibration sequence is required. The calibration process contains two steps to find two calibration parameters: the range multiplier M_R and the gain error correction factor G_{Err}. As the name suggests, M_R is a digital code factor between high and low resistance range and G_{Err} is to compensate for the gain error nonlinearity similar to an ADC. The calibration process is illustrated in Figure 4.36. The average of the digital code ratios between low and high resistance modes at the maximum and the minimum resistances (200kΩ and 100kΩ) in the overlap region is defined as M_R. After the two sub-ranges are aligned to each other with M_R, the maximum and the minimum resistances of the full range (31.6Ω and 200MΩ) are measured. Then, data points at 31.6Ω, 100kΩ, and 200MΩ are normalized by the actual resistance value and analyzed by linear regression. G_{Err} is defined as the slope divided by the y-axis intercept value R_{nom}, the so-called normalization factor. Finally, the resistance can be expressed in terms of digital code, M_R, G_{Err}, and R_{nom}.

$$\text{Resistance}(\Omega) = \frac{\text{Code} \times \{M_R, 1\} \times (1 - \frac{\text{Code}}{R_{nom}} \times G_{Err} \times \{M_R, 1\})}{R_{nom}} \tag{4.23}$$

where $\{M_R,1\}$ is a measurement mode dependent value. Totally, four measurement points are required for calibration. The number obtained in the end is essentially the resistance value, and thus, an absolute error instead of a relative error is shown in Figure 4.34. The linearity error is <±0.8% from 31.6Ω to 200MΩ. It should be noted that the Agilent 34401A multi-meter also contributes linearity error (±0.01% up to 1MΩ, ±0.04% from 1 MΩ - 10MΩ, and ±0.8% above 10MΩ) [119], which means the proposed interface may exhibit better performance than the measured data in Figure 4.34.

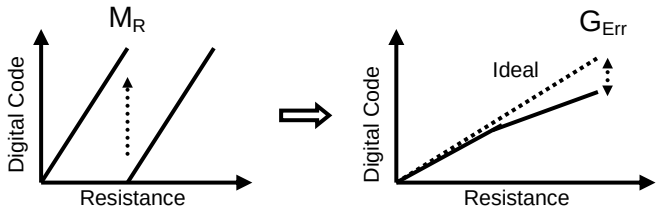


Figure 4.37: Illustration of two-step calibration.

For capacitance the capacitance measurements, no range-to-range calibration but an offset removal is necessary. The digital code associated with the offset capacitance can be simply acquired without external capacitor. A capacitance normalization factor C_{nom} (code per pF) can be calculated by applying a known capacitor and measuring the increment code.

$$\text{Capacitance(pF)} = \frac{\text{Code} - \text{offset}}{C_{nom}} \tag{4.24}$$

The measurements displayed in Figure 4.35 shows a nonlinearity <±0.2% from 0.1pF to 1nF. The Agilent 4284A LCR meter has accuracy depending on capacitance. In the range from 0.1pF to 1nF, it lies between 0.05-0.1% with a $1V_{RMS}$ and 1kHz test signal [120]. Additional errors may come from the frequency dependency of capacitance. The ZPC converts capacitance around 30 (with a 1nF capacitor) to 50 (with a 0.1pF capacitor) times per second, while a 1kHz test signal was used in the LCR meter to obtain a SNR at least 60dB (i.e., 0.1% fluctuation).

Finally, the measured circuit characteristics are compared with the defined specifications in Chapter 2. All results meet the specifications. The dynamic range is limited by SNR and not by linearity. In resistance measurement mode, 40dB SNR can be achieved in the range of 31.6Ω to 200MΩ with a nonlinearity smaller than ±0.8%, corre-

sponding to a 176dB DR. In capacitance measurement mode, 40dB SNR can be achieved in the range of 0.8pF to 1nF with nonlinearity smaller than ±0.2%, corresponding to a 102dB DR. The average current consumed by the circuit is measured to be 32.7μA with a Keithley 6487 picoammeter. Using a 2.5V supply, this translates into an average power consumption of 81.8μW.

Table 4.3: Comparison of specifications and measurement results.

	Specifications	**Fabricated Circuit**
Power	<100μW	81.8μW
Readout Rate	~1Hz	1Hz
Resistance DR	160dB (100Ω - 100MΩ, <±1% error)	176dB (31.6Ω - 200MΩ, <±0.8% error)
Capacitance DR	100dB (1pF - 1nF, <±1% error)	102dB (0.8pF - 1nF, <±0.2% error)
SNR	40dB	>42.5dB
Special Issues	1/f noise, polarization	Pseudo-AC (Chopper)

CHAPTER 5

VERSATILE CHEMICAL FIELD-EFFECT TRANSISTOR INTERFACE

This chapter discusses a versatile interface circuit developed measuring ChemFET characteristics. In the first sub-chapter, design specifications and possible implementations are reviewed. Next, in Chapter 5.2, the proposed low-power measurement scheme and the associated system design will be described. To reduce power consumption, an efficiency analysis of the most power-hungry system components is given in Chapter 5.3. Subsequently, the proposed body-guarded analog switch (BG-switch), which is used in the interface system, is analyzed. Finally, the full system is characterized and the performance is compared with the specifications established in Chapter 2.

5.1 System Level Requirement

As discussed in Chapter 2, none of the interface circuits being proposed for ChemFETs is able to supply voltages beyond chip V_{DD}. Generating high voltages with ICs is not a new concept and can be easily realized with charge pumps or inductor-based DC-DC converters. However, efficiently measuring I_{DS} or V_{GS} with on-chip high-voltage generators is a challenge. Within the defined specifications, applying a continuous I_{DS} = 10μA at V_{DS} = 10V already consumes the maximum power budget of 100μW. Although duty-cycled operation is applicable as the readout rate is only 1Hz, the DC-DC converter loss great amount of energy through ChemFET in each measurement cycle before stabilizing at regulated voltage from initially idle state since the ChemFET keeps draining

current when the converter tries to supply voltage. Fast switching can shorten the stabilization transients, but high switching frequencies increase the gate-drive loss and the oscillator power consumption. Furthermore, the associated switching noise also makes I_{DS} and V_{GS} noisy, reducing the system resolution. Without switching noise, achieving the defined drain current (<±1%) and threshold voltage (<±10mV) resolution is usually not a significant challenge, and has been realized in some of the monolithic ISFET systems introduced in Chapter 2.

Unfortunately, switching DC-DC converters, either capacitor-based or resistor-based, are unavoidable for boosting voltages. Our approach begins with selecting suitable converters for gate and drain biases. Then, by manipulating the control of the converters and the readout strategy, a low-power and switching-free measurement scheme, discussed in detail in the next sub-chapter, is proposed. Obviously, ChemFETs consume most power via the drain current I_{DS}, while requiring only charges to bias the gate. Thus, an on-chip charge pump and an inductor-based DC-DC boost converter are chosen for gate and drain biases, respectively. If the drain bias is to be supplied with another charge pump, the second charge pump should be composed of multiple large off-chip capacitors and driven by a fast switching clock in order to source sufficient amount of energy, which is what we try to avoid.

5.2 System Overview and Operation

To avoid switching noise, the DC-DC converters connected to drain and gate should be idle when taking I_{DS} or V_{GS} measurements. For the gate terminal, the charge pump simply stops switching and hold charges across the gate-source capacitor. Even

though stopping switching the boost converter causes an immediate drop in V_{DS}, a ChemFET biased in the saturation region behaves as a constant current source, assuming that channel length modulation is negligible, for a time period t_{sat} until V_{DS} drops below saturation voltage $V_{DS(sat)}$. If t_{sat}, which can be increased by placing a large regulating capacitor at the output of the boost converter, is long enough, a measurement can be taken within t_{sat}. This way, switching free measurement is realized, but the long boost converter transient, which causes a substantial energy loss, is still a significant concern. The ultimate reason is that the ChemFET keeps draining current even before V_{DS} reaches the target voltage. Hence, one simple way to decrease the transient time during which I_{DS} is non-zero is to disable the ChemFET when the boost converter is charging the output capacitor. This whole idea is illustrated in Figure 5.1.

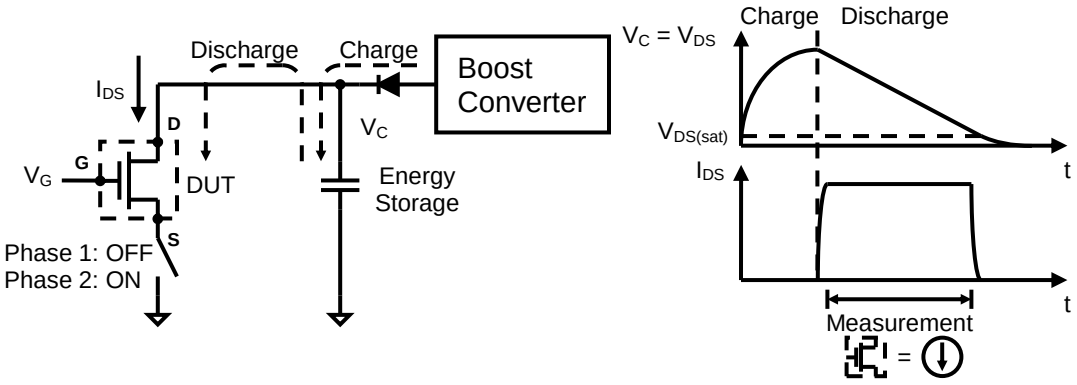


Figure 5.1: Illustration of drain biasing scheme and associated V_{DS} and I_{DS} waveforms. The measurement period is exaggerated in the waveform plot.

The operation is divided into two phases. In phase 1, the boost converter charges the output capacitor, which is now called energy storage capacitor C_{EG}, and a switch connected to the source of the ChemFET is kept open to ensure $I_{DS} = 0$ (i.e., no energy

loss through the device under test (DUT)). In phase 2, assuming that sufficient gate voltage is applied, the boost converter is turned off and the switch is closed to discharge C_{EG} through the DUT. During the discharge phase (see timing diagram in Figure 5.1), the voltage across C_{EG} will decrease linearly with approximately constant I_{DS} as long as the ChemFET remains biased in saturation region. If a current measurement is always taken with the same time delay t_d after the initiation of the discharge process, the measured current non-linearity is not significant. Because of channel length modulation, the I_{DS} measured after t_d is lower than the drain current I_{DS0} at the beginning of discharge phase. If ΔV_D represents the voltage drop during the discharge process, ΔV_D after the time t_d can be derived as,

$$\Delta V_D = \frac{t_d I_{DS0}}{C_{EG} + \lambda t_d I_{DS0}} \tag{5.1}$$

where λ is channel length modulation factor. Note that ΔV_D is not simply $t_d I_{DS0}/C_{EG}$ because the channel length modulation is also a function of ΔV_D. As a result, the actual drain current being applied at t_d becomes,

$$I_D = I_{DS0}\left(1 - \frac{\lambda t_d I_{DS0}}{C_{EG} + \lambda t_d I_{DS0}}\right) = I_{DS0} F_{CH} \tag{5.2}$$

where F_{CH} denotes a factor between the measured I_D and the I_{DS0}. If F_{CH} would be a constant, the actual measurement current applied at time t_d would always be the same fraction of I_{DS0}, even if I_{DSO} changes. Thus, changes in I_{DS0} could be appropriately monitored by measuring I_d at time t_d. However, F_{CH} is a function of I_{DS0}, introducing a non-linearity in the relation between I_D and I_{DS0}. This non-linearity can be expressed by the sensitivity F_{CH} to changes in I_{DS0} as follows,

$$\frac{\Delta F_{CH}}{F_{CH}} = -\frac{\lambda t_d I_{DS0}}{C_{EG} + \lambda t_d I_{DS0}} \frac{\Delta I_{DS0}}{I_{DS0}} \tag{5.3}$$

Using reasonable numbers, C_{EG} = 3.3nF, t_d = 1ms, I_{DS0} = 10μA, and λ = 0.005V^{-1} (the channel length modulation factor measured for a 5μm channel length IGZO TFT), a large 10% I_{DS0} change results in only a 0.15% change in F_{CH}, i.e., a 0.15% nonlinearity. Using long channel ChemFETs, short delay times, low biasing currents, and large energy-storage capacitors the linearity can be further improved.

The complete ChemFET interface that utilizes the measurement scheme proposed in Figure 5.1 is shown in Figure 5.2. The system provides external digital control of gate and drain bias voltages, but the readout signals, I_{DS} and V_{GS}, are only analog. To increase flexibility, the system is made highly reconfigurable by breaking it up into individual system blocks. Depending on the desired operation mode, each block can be re-routed in a package through bonding wires or on a PCB with switches. Note that not all off-chip components are shown in Figure 5.2.

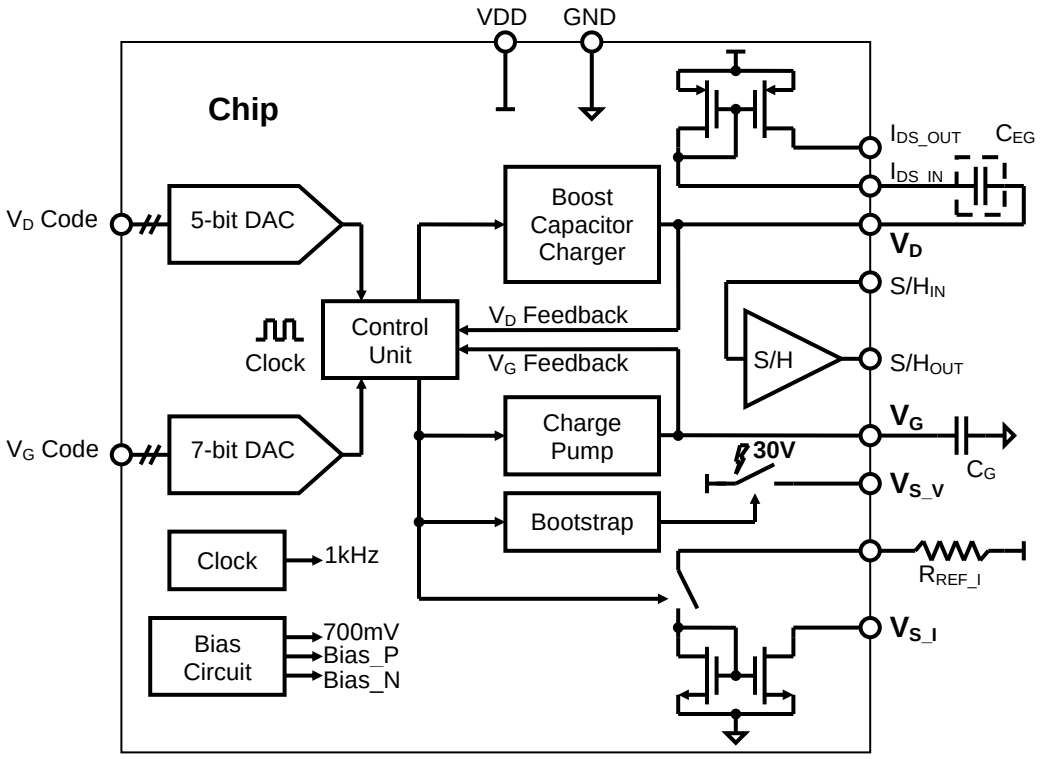


Figure 5.2: The rectangular box denotes the boundary between on-chip and off-chip components. Corresponding connections of ChemFET to the interface in different measurement modes are described in Table 5.1.

A 5-bit DAC controls drain voltage up to 13V with a resolution of 0.5V/LSB and a 7-bit DAC controls gate voltages up to 6.44V with 70mV/LSB resolution (the values are based on measurement results). The output voltages of boost capacitor charger and charge pump are compared to digitally assigned values through feedback networks to regulate V_D and V_G, respectively. All bias voltages as well as a voltage reference are generated on chip. A slow system clock (1kHz) is generated with a relaxation oscillator for low power operation. The detail system operation depends on the measurement mode and signal routing.

In constant voltage mode, both DC-DC converters are activated to charge up V_D and V_G at the beginning of each measurement cycle until they reach their target values.

The converter that finishes charging first is simply deactivated and holds charges until the other converter reaches its target voltage. The boost converter charges C_{EG} through the body diode of a P-mirror into V_{DD} and automatically disables the mirror. A loading capacitor is placed at the output of the charge pump for two reasons: (1) to reduce the voltage step for each charging cycle in order to improve the V_G accuracy and (2) to avoid a V_G drop caused by the discharging switch. The ChemFET source is connected to the terminal V_{S_V} to discharge C_{EG} into V_{DD}. Referencing the ChemFET source to V_{DD} instead of ground is because of the "boost" characteristic of the charge pump and the capacitor charger, which only generate voltages above V_{DD}. Hence, a bootstrap circuit is required for driving the discharge switch. The discharge current will be redirected to I_{DS_OUT} through a P-mirror and a load resistor can be connected to the I_{DS_OUT} terminal to convert the current into a voltage. Since the current (or the voltage) is only a short pulse, the input of a sample-and-hold (S/H) amplifier employing an ultra-low leakage technique (described in Chapter 5.4) can be connected to I_{DS_OUT} terminal to hold the readout value, Thereby, the read out is synchronized with the discharge signal with a fixed time delay t_d = 1ms.

In constant current mode, the ChemFET source has to be connected to a current sink terminal V_{S_I}. The desired I_{DS} can be adjusted by an external resistor R_{REF_I}. To obtain the variation in V_T, V_S is measured at a fixed V_G, and thus, V_{S_I} is connected to the input of the S/H amplifier. One of the advantages of the constant current mode is its immunity to non-linearity because I_{DS0} in (5.3) is always a constant.

Although the design and characterization of the interface focuses on the constant voltage and constant current modes, additional sub-modes can be realized with the pro-

posed interface. If high voltage operation is not necessary, one or both converters can be disabled by assigning zero V_D and/or V_G code(s) to save power. In these cases, we can take advantage of the constant V_{DD} to bias the ChemFETs with proper signal routings. In Table 5.1, all possible situations and their corresponding routings are listed. Note that different restrictions are applied in different modes (e.g., $V_{S\_I} < V_{DD}$ due to the input common mode range of the S/H amplifier). Maximum attainable V_{GS} and V_{DS} may also vary according to the selected mode.

Table 5.1: Detail applicable operation modes with associated signal routing and DC-DC converter activation.

Mode		Routing/Activation						
		ChemFET				S/H_{IN}	Boost Converter	Charge Pump
		G	S	D	Region			
Constant Voltage		V_G	V_{S_V}	V_D	Sat./ Triode	I_{DS_OUT}	X	X
Constant Current	$V_{GS}\geq V_{DD}$ $V_{DS}\geq V_{DD}$	V_G	V_{S_I}	V_D	Sat./ Triode	V_{S_I} ($V_{S\_I}<V_{DD}$)	X	X
	$V_{GS}<V_{DD}$ $V_{DS}\geq V_{DD}$	V_{DD}	V_{S_I}	V_D	Sat.	V_{S_I}	X	
	$V_{GS}<V_{DD}$ $V_{DS}<V_{DD}$	V_{DD}	V_{S_I}	V_{DD}	Sat.	V_{S_I}		

5.3 Pulse-activated Boost Capacitor Charger Analysis

Among the various blocks in the proposed interface system, the boost capacitor charger consumes the majority of the system power as it charges a large C_{EG} (usually in ~nF) to provide enough energy for the discharge period. Hence, the efficiency of the boost capacitor charger strongly affects the total power consumption. The design and behavior of PCB-based high-power high-voltage (>1kV) capacitor chargers based on resonant or boost converter architecture have been discussed [121-123]; however, the effi-

ciency analysis, especially for integrated converters, has not yet been done. Moreover, we pulse the boost converter instead of using conventional duty-cycle control because of the slow system clock (1kHz).

The schematic of the pulse-activated boost capacitor charger is shown in Figure 5.3. Except for the inductor, C_{EG}, C_{FB1}, and ChemFET (DUT), all components are implemented on chip. The region circled by the dashed box is essentially a boost converter. The inductor is energized by pulsing SW_L and de-energized through C_{EG} and the annotated body diode in the current mirror. To regulate the drain voltage without losing charges in C_{EG}, the charger employs a capacitively coupled feedback network consisting of a voltage divider (C_{FB1} and C_{FB2}) and two switches (SW_{F1} and SW_{F2}). Voltages across C_{FB1} and C_{FB2} are respectively reset to zero and V_{DD} at the beginning of each charging cycle so that the feedback voltage with respect to ground will be a factor of the voltage increase at the converter output (ChemFET drain).

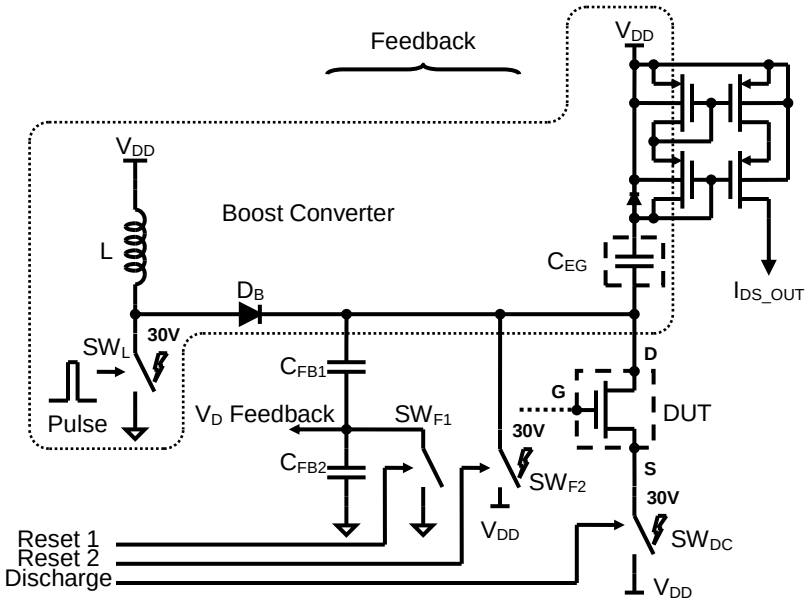


Figure 5.3: Schematic of the pulse-activated boost capacitor charger. Components in the dashed box form a boost converter. Other components are ChemFET and supporting control circuits.

The first three cycles of the inductor current I_L and C_{EG} voltage V_C waveforms are shown in Figure 5.4. Φ_1 and Φ_2 denote the energizing and de-energizing phases of the inductor, respectively, where the duration of Φ_1 is essentially the pulsewidth t_{PL}. The pulse is synchronized with the 1kHz system clock and the pulsewidth is adjustable using an external resistor. $V_{C,n}$ denotes the final V_C after the nth de-energizing cycle.

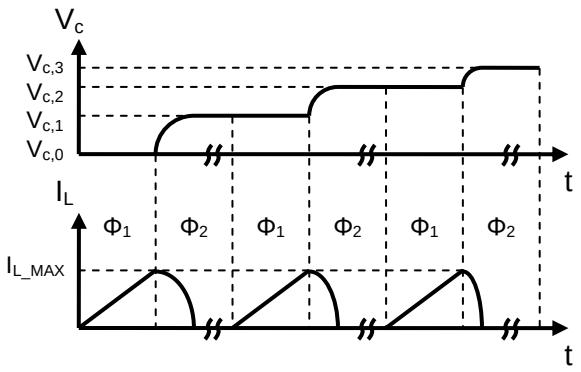


Figure 5.4: Inductor current and capacitor voltage waveforms. $V_{C,n}$ denotes the ultimate capacitor voltage after nth energizing/de-energizing cycle.

The power loss mechanisms in the proposed charger include diode loss, resistive loss, and ringing loss. Each mechanism will be analyzed separately by assuming the other two losses are negligible. Because the increase of the capacitor voltage is a highly non-linear recurrance process, the losses are not constant either from cycle to cycle; thus, a number of assumption and approximation are made to simplify the analysis. The purpose of the analysis is not to accurately determine the absolute energy losses, but instead, we try to understand the behavior of each loss mechanism as a function of the operation parameters (e.g., pulsewidth).

To aid the following analysis, measured values of device parameters in the boost capacitor charger are listed in Table 5.2.

Table 5.2: Measured device values (ranges) of boost capacitor charger.

Parameter	Symbol	Value (Range)
Inductance	L	80μH
Inductor serial resistance	R_{ESR_L}	1.4Ω
Switch resistance	R_{SW}	61.2Ω
Energy storage	C_{EG}	3.3nF
Drain parasitic capacitance of switch	C_{par}	9.7pF
Total diode forward bias voltage	V_D	1.6V
Driving pulsewidth	t_{PL}	100-1000ns
Maximum inductor current	I_{L_MAX}	4.24-27.4mA

5.3.1 Diode Loss

The diode loss is analyzed only in phase Φ_2 because there is no diode involved in phase Φ_1. The simplified circuit schematic and current flow diagram associated with diode loss is shown in Figure 5.5. Because of conservation of energy, the energy stored in the inductor E_{ind} will be either dissipated in D_B and D_{Body} or transferred to C_{EG}. Thus, the energy stored in the inductor E_{ind} can be written as,

$$E_{ind} = V_D \int_0^{t_{off}} I_L(n,t)\,dt + \frac{1}{2} C_{EG}\left(V_{C,n}{}^2 - V_{C,n-1}{}^2\right) \tag{5.4}$$

$$= C_{EG} V_D \left(V_{C,n} - V_{C,n-1}\right) + \frac{1}{2} C_{EG}\left(V_{C,n}{}^2 - V_{C,n-1}{}^2\right) \tag{5.5}$$

where t_{off} is the time when the inductor current drops to zero and $I_L(n,t)$ the inductor current as a function of time and cycle number n. The first term of (5.4) and (5.5) represents the diode loss, while the second term is the energy being transferred to the capacitor. Hence, the transfer efficiency of the n-th cycle is,

$$\eta_{D2}(n) = \frac{V_{C,n} + V_{C,n-1}}{V_{C,n} + V_{C,n-1} + 2V_D} \tag{5.6}$$

(5.6) implies that the efficiency depends only on the initial and final voltages of the nth cycle and increases with n. Intuitively, this is because, in Figure 5.4, the diode loss is es-

sentially the product of V_D and the area below $I_L(n,t)$ in Φ_2 which decreases with n. This is because the $V_{C,n}$ increases with n and, thus, $I_L(n,t)$ drops even faster. By summing the loss over n cycles with $V_{C,0} = 0$, the total loss in the diode can be found,

$$\mathrm{Loss}_{D2} = \sum_{k=1}^{n} C_{EG} V_D \left(V_{C,k} - V_{C,k-1}\right) = C_{EG} V_D V_{C,n} \tag{5.7}$$

and the overall efficiency becomes,

$$\eta_{D2} = \frac{V_{C,n}}{V_{C,n} + 2V_D} \tag{5.8}$$

(5.7) and (5.8) state that the total diode loss and the overall efficiency depend only on the final targeted capacitor voltage. The efficiency increases with the target voltage. Intuitively, the diode loss is proportional to the total charge flow through the diodes and the total charge is only related to the capacitor voltage. Thus, the efficiency (or loss) is only a function of capacitor voltage. For the maximum $V_C = 13V$ in the proposed interface and a simulated V_D around 1.6V, the best attainable circuit efficiency without considering other loss mechanisms is 80.2%.

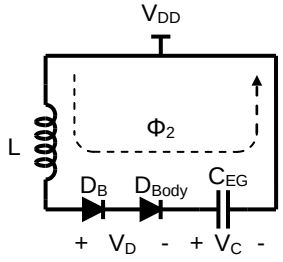


Figure 5.5: Simplified circuit and signal flow used for analyzing diode loss in de-energizing phase.

5.3.2 Resistive Loss

The resistive losses during the energizing phase are caused by the inductor series resistance R_{ESR_L} and the switch resistance R_{SW}, as is illustrated in Figure 5.6. Assuming a short energizing period (i.e., $t_{PL} << L/(R_{ESR\_L} + R_{SW})$), the inductor current increases linearly with time until t_{PL}. The total energy loss after n cycles is n times the loss in one cycle and can be easily derived as,

$$\begin{aligned} \mathrm{Loss_{R1}} &= \mathrm{n}\left(\mathrm{R_{ESR\_L}} + \mathrm{R_{SW}}\right)\int_0^{\mathrm{t_{PL}}}\left(\frac{\mathrm{V_{DD}}}{\mathrm{L}}\mathrm{t}\right)^2 \mathrm{dt} = \mathrm{n}\frac{{\mathrm{V_{DD}}}^2}{3\mathrm{L}^2}\left(\mathrm{R_{ESR\_L}} + \mathrm{R_{SW}}\right){\mathrm{t_{PL}}}^3 \\ &\propto \mathrm{t_{PL}} \end{aligned} \tag{5.9}$$

In (5.9), n and t_{PL} are mutually related parameters. The amount of energy stored in the inductor is proportional to ${t_{PL}}^2$ and, thus, for a given V_C (i.e., capacitor energy), n is inversely proportional to ${t_{PL}}^2$. Hence, the $Loss_{R1}$ is effectively proportional to t_{PL}.

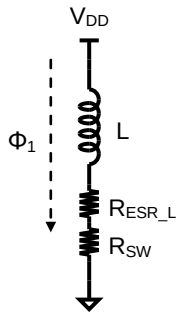


Figure 5.6: Simplified circuit and signal flow used for analyzing resistive loss in the energizing phase.

Analyzing resistive losses in the de-energizing phase is more difficult because I_L is essentially part of a damped resonating waveform (Figure 5.7). A straightforward way is to solve the second order differential equation to find $I_L(n,t)$ and integrate the product

of equivalent series resistor (R_{ESR_L} and diode resistance) and $I_L^2(n,t)$ from t = 0 to t = t_{off}. However, in this work we are more looking for a simple expression that helps guide the design towards better efficiency. Thus, instead of solving differential equations, we try to take advantage of the quality factor, which is defined as,

$$Q = 2\pi \frac{\text{Energy stored}}{\text{Energy dissipated per cycle}} \tag{5.10}$$

Assuming R_{ESR_L} is small and the change of the resonant frequency due to R_{ESR_L} is negligible, the energy dissipated in every quarter-cycle is the same. Now, the total energy stored in the circuit is the energy stored in the inductor, the capacitor, and the pseudo energy stored in the two diodes. The diode voltage drop (similar to a battery) can be interpreted as a pre-charge voltage across C_{EG}. This way, energy is exchanged between the inductor and the capacitor, and the de-energizing current can be viewed as part of resonance current starting at -π/2 at a pseudo I_L level I_{EQ}, which essentially describes the current waveform needed to move all energy back into the inductor (Figure 5.7(b)). Thus, the following energy balance holds:

$$\frac{1}{2} L I_{EQ,n}{}^2 = \frac{1}{2} L I_{L\_MAX}{}^2 + \frac{1}{2} C_{EG} (V_D + V_{C,n})^2 \tag{5.10}$$

In Figure 5.7(b), the region from -t_0 to 0 essentially describes the de-energizing waveform in Figure 5.4 with $I_{L\_MAX} = I_{EQ} \sin(t_0)$.

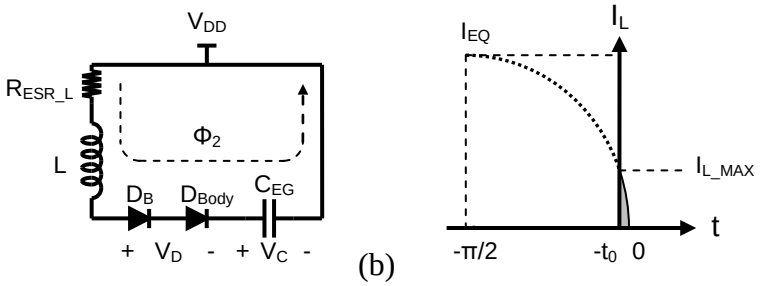


Figure 5.7: (a) simplified circuit, signal flow, and (b) pseudo inductor current concept used for analyzing resistive loss during the de-energizing phase.

The ratio of the energy dissipated from $-t_0$ to 0 compared to the dissipation in a quarter cycle ($-\pi/2$ to 0) can be expressed as,

$$\frac{\text{Dissipation}\ (-t_0, 0)}{\text{Dissipation}\ (-\pi/2, 0)} = \frac{\int_0^{t_0} \sin^2(t)dt}{\int_0^{\pi/2} \sin^2(t)dt} = \frac{2}{\pi}[t_0 - \text{Cos}(t_0)\text{Sin}(t_0)]$$
$$= \frac{2}{\pi}\left(\text{Sin}^{-1}\frac{I_{L\_MAX}}{I_{EQ,n}} - \frac{I_{L\_MAX}}{I_{EQ,n}}\sqrt{1 - \frac{{I_{L\_MAX}}^2}{{I_{EQ,n}}^2}}\right) \quad (5.11)$$

(5.11) can be further simplified since $I_{L\_MAX} << I_{EQ}$ except for the first few de-energizing cycles. This assumption is valid as, after a few charging cycles, the total energy stored in the circuit is generally large compared to the energy added into each cycle. Finally, (5.11) becomes,

$$\frac{\text{Dissipation}\ (-t_0, 0)}{\text{Dissipation}\ (-\pi/2, 0)} = \frac{1}{\pi}\frac{{I_{L\_MAX}}^3}{{I_{EQ,n}}^3} \quad (5.12)$$

Thus, the total energy loss becomes,

$$\text{Loss}_{R2} = \sum_n \frac{\text{Dissipation}\ (-\pi/2, 0) \times \text{Dissipation}\ (-t_0, 0)}{\text{Dissipation}\ (-\pi/2, 0)}$$
$$= \sum_{k=0}^{n} \frac{\pi L {I_{EQ,k}}^2}{4Q} \times \frac{1}{\pi}\frac{{I_{L\_MAX}}^3}{{I_{EQ,k}}^3} = \sum_{k=0}^{n} \frac{L{I_{L\_MAX}}^3}{4QI_{EQ,k}} \quad (5.13)$$

Where the total dissipation from –p/2 to 0 equals ¼ times the total stored energy $LI_{EQ,k}^2$ divided by the Q-factor. We can see that the energy dissipation in a single cycle decreases with n since $I_{EQ.n}$ increases with n. Intuitively speaking, it is again because the area underneath $I_L(n,t)$ in Φ_2 decreases with n (Figure 5.4). The term $I_{L\_MAX}^3$ is proportional to t_{PL}^3. By substituting $I_{EQ.n}$ with (5.10) and using the assumption that the stored energy in the capacitor is larger than the energy stored in the inductor in each cycle,

$$\mathrm{Loss}_{R2} \propto \sum_{k=0}^{n} \frac{t_{PL}^3}{I_{EQ,k}} = \sum_{k=0}^{n} \frac{t_{PL}^3}{\sqrt{I_{L\_MAX}^2 + \frac{C_{EG}}{L}(V_D + V_{C,k})^2}} \cong \sum_{k=0}^{n} \sqrt{\frac{L}{C_{EG}}} \frac{t_{PL}^3}{V_D + V_{C,k}} \qquad (5.14)$$

With a fixed target V_C, an increase n effectively adds terms to the summation. If we consider an equally spaced $V_{C,n}$ series (in reality, $V_{C,n} - V_{C,n-1}$ becomes smaller for increasing n), the summation in (5.14) can be simplified as,

$$\sum_{k=0}^{n} \frac{t_{PL}^3}{V_D + \frac{kV_C}{n}} \propto n \qquad (5.15)$$

because the derivative of the summation in (5.15) with respect to n yields several terms of poly gamma function, which is roughly a constant (±1% if n > 3). Thus, the total resistive loss in Φ_2 is,

$$\mathrm{Loss}_{R2} \propto n \times t_{PL}^3 \propto t_{PL} \qquad (5.15)$$

It is not surprising that (5.15) yields the same behavior as the resistive loss in Φ_1 since, except for the first few cycles, $I_L(n,t)$ varies approx. linearly with time in both Φ_1 and Φ_2. In fact, the resistive loss in Φ_2 is much smaller than in Φ_1 because the series resistance measured in Φ_1 ($R_{ESR\_L} + R_{SW} = 62.6\Omega$) is much larger than that in Φ_2 ($R_{ESR\_L} = 1.4\Omega$). Ultimately, we can conclude that the overall resistive loss is proportional to t_{PL}.

$$\text{Loss}_R \propto t_{PL} \tag{5.16}$$

5.3.3 Ringing Loss

The ringing loss mechanism is illustrated in Figure 5.8. At the beginning of Φ_2, $I_L(n,t)$ charges a parasitic capacitor C_{par} from approx. 0 to $V_D + V_{C,n-1}$ before charging C_{EG}. When $I_L(n,t)$ drops to zero at the end of Φ_2, the voltage across C_{par} reaches $V_D + V_{C,n}$. The energy stored in C_{par} is ultimately a loss, called ringing loss [124]. The name comes from the fact that the energy in C_{par} is dissipated through a damped resonance occurring right after $I_L(n,t) = 0$ between L and C_{par} (the oscillation is damped because of parasitic resistances). The ringing dissipates most energy stored in C_{par} and lasts until the voltage across C_{par} becomes V_{DD}; the residual energy ($0.5C_{par}V_{DD}^2$) will be lost in the next energizing cycle. By measuring the ringing period of the developed circuit, C_{par} is found to be 9.7pF. C_{par} consists of pad, leads package, PCB, and diode parasitic capacitances, as well as drain-gate and drain-body capacitance (n-well-body p-n junction) of the drain-extended MOSFET (DEMOS) switch. A screen capture of the measured inductor current through several ringing cycles is shown in Figure 5.9.

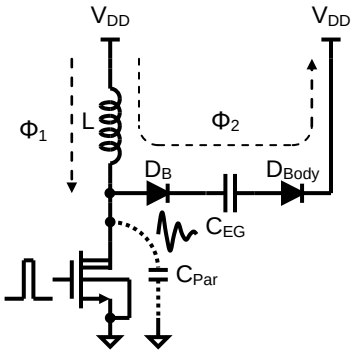


Figure 5.8: Equivalent circuit and signal flow used for analyzing ringing loss.

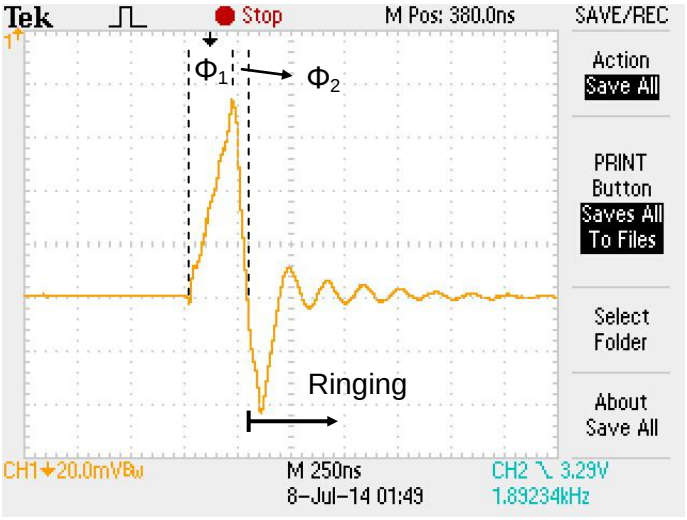


Figure 5.9: Oscilloscope screen capture of inductor current (measured with a small resistance in series with circuit and supply voltage) in boost capacitor charger including energizing phase Φ_1, de-energizing phase Φ_2, and subsequent ringing phase.

The total ringing loss is the summation of the maximum energy being stored in C_{par} in each cycle, as charging C_{par} with L only incurs small resistive losses associated with R_{ESR_L}.

$$\mathrm{Loss_{Ring}} = \sum_{k=1}^{n} \frac{1}{2} C_{par} \left(V_D + V_{C,k}\right)^2 = \frac{1}{2} C_{par} \left(n V_D + \sum_{n} {V_{C,n}}^2 + 2 V_D \sum_{n} V_{C,n} \right) \quad (5.17)$$

To evaluate (5.17), we sum both sides of the energy conservation equation (5.5) over n cycles,

$$n \frac{1}{2} L {I_{L\_MAX}}^2 = C_{EG} V_D \left(\sum_{n} V_{C,n} - \sum_{n} V_{C,n-1} \right) + \frac{1}{2} C_{EG} \left(\sum_{n} {V_{C,n}}^2 - \sum_{n} {V_{C,n-1}}^2 \right) \quad (5.18)$$

(5.18) can be simplified as,

$$n L {I_{L\_MAX}}^2 = 2 C_{EG} V_D V_{C,n} + C_{EG} {V_{C,n}}^2 \quad (5.19)$$

Summing (5.19) again over n cycles yields,

$$2V_D \sum_n V_{C,n} + \sum_n {V_{C,n}}^2 = \frac{n(n+1)}{2} \frac{L{I_{L\_MAX}}^2}{C_{EG}} \tag{5.20}$$

Substituting (5.17) with (5.20) yields,

$$Loss_{Ring} = \frac{1}{2} C_{par} \left(nV_D + \frac{n(n+1)}{2} \frac{L{I_{L\_MAX}}^2}{C_{EG}} \right) \cong \frac{1}{2} C_{par} \frac{n^2}{2} \frac{L{I_{L\_MAX}}^2}{C_{EG}} \tag{5.21}$$

In (5.21), the coefficients of the n and n^2 terms are of the same order and, thus, the n^2 term dominates the ringing loss as it increases much faster than n. Because n and I_{L_MAX} are, respectively, proportional to ${t_{PL}}^{-2}$ and t_{PL}, we can conclude that the ringing loss is,

$$Loss_{Ring} \propto n^2 {I_{L\_MAX}}^2 \propto \frac{1}{{t_{PL}}^2} \tag{5.22}$$

(5.22) states that the ringing loss can approach infinite if t_{PL} is extremely short. In fact, if t_{PL} is too short to energize the inductor with sufficient energy to charge C_{par} to V_{DD} + $V_{C,n-1}$, the overall efficiency will become zero. Intuitively, (5.22) means that if a short t_{PL} is chosen, more cycles are needed to charge C_{EG} to the same value, and thus, ringing and the associated loss occur more often.

5.3.4 Total Loss

After analyzing individual the loss mechanisms, the dependence of diode, resistive, ringing, and total losses on the pulsewidth can be shown on the same graph (Figure 5.10). It should be emphasized that this figure is solely conceptual and not drawn to scale. With the efficiency being inversely proportional to the system losses, the minimum in the total loss yields the optimum t_{PL} to obtain maximum efficiency.

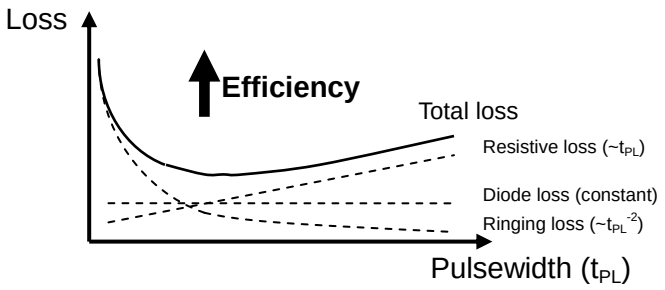


Figure 5.10: Illustration of diode, resistive, ringing, and total loss as a function of t_{PL}.

The simulation boost capacitor charger efficiency as a function t_{PL} for different target V_C is shown in a 3D graph in Figure 5.11. Clearly, a region yielding maximum efficiencies (the blue ridgeline) can be seen at t_{PL} around 300ns to 400ns for V_C from 4V to 13V. The decrease in efficiency is due to the increase in resistive losses when t_{PL} is >400ns and the increase in ringing losses when t_{PL} is <400ns. At higher V_C, higher maximum efficiency is achieved because the relative contribution of the diode loss with respect to the overall invested energy decreases. For t_{PL} = 100ns, the maximum achievable V_C is 10V. Points with long t_{PL} at low V_C are not recorded because of large errors (>200mV) between real V_C and targeted V_C caused by discontinuous V_C values. During efficiency calculation, real V_C values instead of targeted V_C are used.

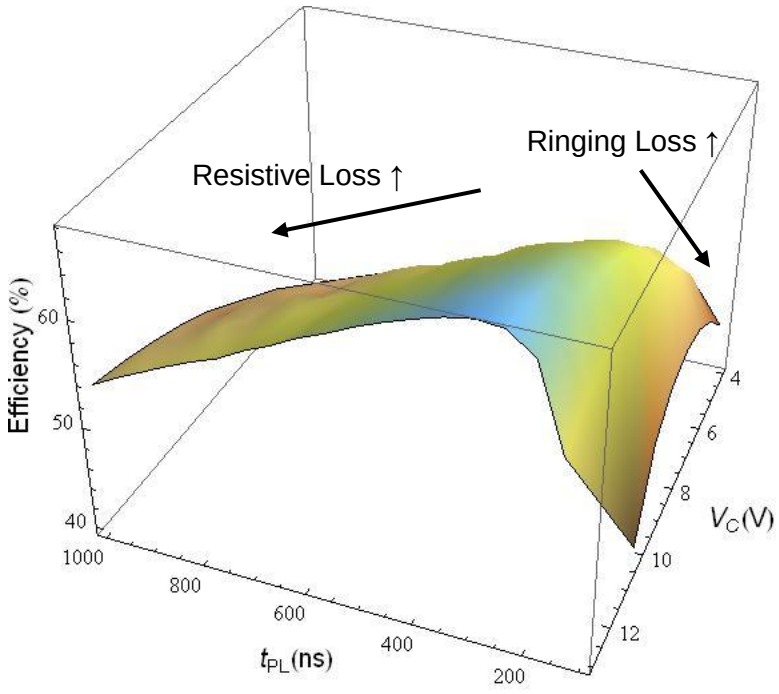


Figure 5.11: Simulated boost capacitor charger efficiency as a function of t_{PL} and V_C.

5.4 Body-Guarded Switches and Applications

In the proposed interface, switched-capacitor (SC) circuits are widely used for their low power consumption. However, the capacitors in SC circuits begin to lose or gain charges right after every clock edge through imperfect (leaky) switches and, thus, clock periods induce voltage errors, especially for our low-speed system, unless large capacitors are used. Hence, we propose a low-leakage body-guarded switch (BG-switch) technique to improve voltage accuracy. BG-switches are used at the output of the charge pump and in the S/H amplifier in the ChemFET interface. Replicated circuit blocks were fabricated together with the same circuits employing conventional CMOS transmission gates on a separated chip (Figure 5.12) to compare their performance. An additional application, an SC amplifier, is also demonstrated on the same chip.

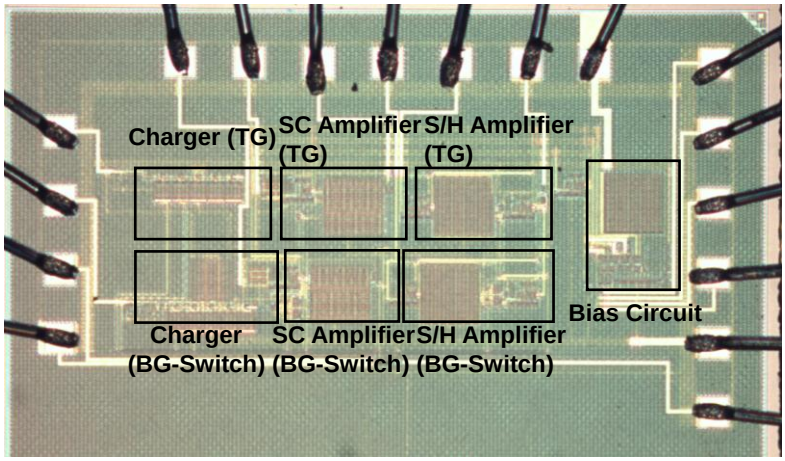


Figure 5.12: Microscope image of the chip containing BG-switch enabled test circuits as well as test circuits using conventional transmission gates, fabricated in 0.35µm Texas Instrument BiCMOS process. The die size is 2mm × 1mm.

In standard process technologies, MOSFETs are often used as analog switches, and MOSFET off-state leakage currents often dominate the SC circuit leakage, while the leakage of the capacitor itself can be ignored. MOSFET leakage currents cannot be treated as a switch imperfection similar to charge injection phenomena and, thus, cannot be mitigated with fully-differential SC circuits [125]. In practice, the error in the fully-differential architecture could even increase when two capacitors holding opposite half signals are subject to leakage currents in opposite directions.

As depicted in Figure 5.13, the leakage current in an off-state MOSFET consists of gate leakage (I_G), subthreshold leakage (I_{SVT}), punchthrough current (I_{PUN}), gate-induced drain leakage (I_{GIDL}), and p-n junction reverse-biased current (I_{REV}) [126]. The magnitude and relative contribution of each leakage source strongly depend on the fabrication process [127]. Considering the applications in low-speed SC circuits, we focus here on leakage reduction in a mature, commercial 0.35µm BiCMOS process. With gate oxide thicknesses of typical 0.35µm CMOS processes in the range of 6-8nm [128],

we can neglect I_G in this work compared to other leakage sources [129, 130].

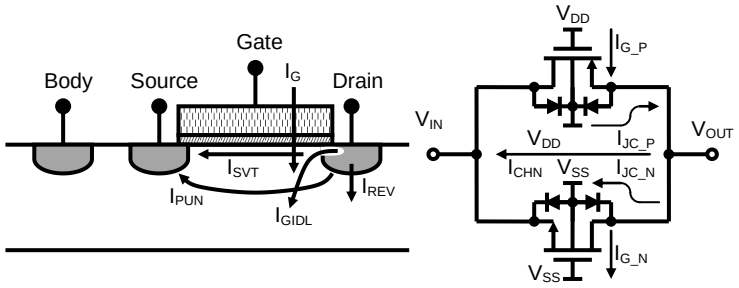


Figure 5.13: Leakage current sources in MOSFETs in (left) device cross-sectional view and (right) transmission gate symbol. In the symbol view, I_{SVT} and I_{PUN} are merged to be I_{CHN} and I_{GIDL} and I_{REV} are merged to be I_{JC_N} or I_{JC_P}.

Engineers became aware of the leakage problem when MOSFETs with sub-micrometer gate length were used for power gating in digital circuits. Using high threshold voltage devices [131, 132] or applying a gate-source underdrive [133, 134] are effective ways to suppress I_{SVT} in power-gating applications. In analog circuits, the gate underdrive technique can be implemented into the analog switches [135] to improve circuit non-linearity caused by switch leakage. However, all leakage currents are a function of the MOSFET terminal voltages and, thus, I_{SVT} may not always be the dominant factor. A solution that takes more leakage sources into account is to inject a compensation current, generated by a switch replica, into the circuit leaky node [136, 137]. This method provides more accurate leakage cancellation, but requires complex circuits and the cancellation efficiency is limited by device mismatch.

The BG-switch technique is inspired by the shielding concept of a triaxial cable, which is used for measuring extremely small currents (Figure 5.14(a)). To solve the problem of dielectric leakage currents of coaxial cables, an inner shield buffered at the

same potential as the inner core is inserted in between inner core and outer shield. This inner shield blocks away any leakage current and redirects it into the buffer. In a MOSFET, the ultimate reason for device leakage is non-zero potential drops across p-n junctions and along the device channel. Consequently, we can mimic the triaxial cable by dynamically biasing the body terminal to force potential drops across junctions to zero and redirect the channel leakage current into the buffer, as long as the switch is in the off state.

The practical implementation of the BG-switch is shown in Figure 5.14(b). When the BG-switch is on, it works like a conventional transmission gate (TG) (i.e., biasing the NMOS body at V_{SS} and the PMOS body at V_{DD}). In the off state, however, the body terminal of the BG-switch is biased at the potential of the leakage sensitive node V_{SEN} through a unity-gain buffer. A TG operating in phase with the BG-switch is appended to avoid forward bias of parasitic diodes in the BG-switch.

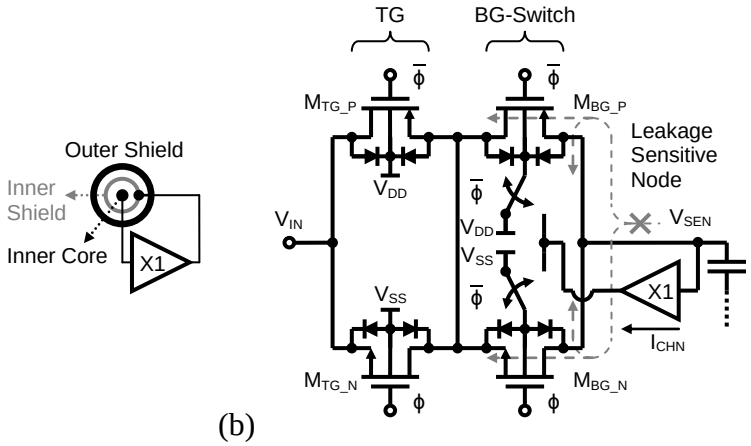


Figure 5.14: (a) Cross section and driving buffer of a triaxial cable. (b) Practical implementation of a BG-switch with MOSFETs. I_{CHN} denotes the total channel leakage current being redirected into the buffer.

In the off state, most of the voltage difference between V_{IN} and the BG-switch body is dropped across the TG. This brings the source of M_{BG_N} and the drain of M_{BG_P} close to V_{SEN}. A gate underdrive hence is automatically formed in the BG-switch to suppress I_{SVT} when V_{SEN} lies between V_{DD} and V_{SS}. I_{SVT} is further reduced because of the decrease of drain induced barrier lowering (DIBL) effect. I_{PUN} is also decreased as the small p-n junction bias reduces the proximity of depletion regions underneath the channel. Furthermore, no matter how large the residual I_{SVT} and I_{PUN}, they will be finally redirected into the buffer (I_{CHN}) without affecting the leakage sensitive node. Finally, I_{GIDL} and I_{REV} are strongly suppressed by reducing the voltage drop across the junction, but a small residual could appear as a result of a buffer offset.

The implementation of a BG-switch requires an isolated NMOS. This is possible in a BiCMOS process since either an n- or p-buried layer is usually available. Considering the layout, the buffer offset should be minimized to reduce the residual I_{GIDL} and I_{REV}. Non-butting body contacts are preferred as they avoid forming highly-doped p-n junctions and reduce band-to-band tunneling (BTBT) currents in I_{REV}. Such layout slightly increases the chance of latch-up, but we can prevent it with a ring body contact and sufficient separation between NMOS and PMOS. Other small residual leakages that cannot be eliminated with BG-switches include the capacitor leakage and edge direct tunneling (EDT) current through the gate oxide.

The simplified BG-switch shown in Figure 5.15 will be used in subsequent SC circuit schematics. The shaded switch has a dynamic body terminal, and V_{BG} is the corresponding second body bias. Not all switches in a SC circuit require the BG technique, but only those that significantly affect charges being held. To use a BG-switch, the first

step is, thus, to determine the critical switches in a circuit.

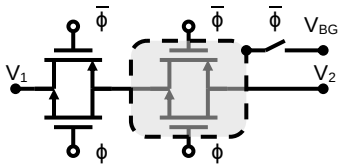


Figure 5.15: Simplified switch with a TG on the left and a BG-switch on the right.

5.4.1 Sample-and-Hold Amplifier

The S/H amplifier shows the most straightforward way to use a BG-switch. As shown in Figure 5.16, the leakage sensitive node is V_{HOLD} and the amplifier itself can apparently serve as the unity-gain buffer. In the chip implementation, V_{IN} is further buffered by an on-chip unity gain buffer. As leakage current is usually not a well-modeled parameter, simulation do not show reliable results for the effect of the BG-switch. Consequently, a large (C_{HOLD} = 11.99pF) poly-poly capacitor is chosen to ensure that the observation time of the V_{OUT} change is sufficient over a wide temperature range.

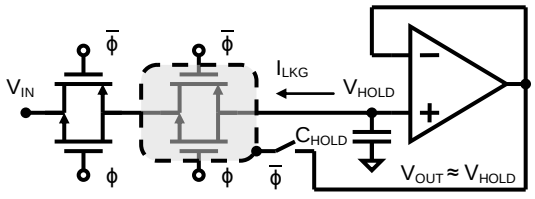


Figure 5.16: Schematic of sample-and-hold amplifier employing BG-switch. I_{LKG} denotes switch leakage flowing through C_{HOLD}.

The leakage current I_{LKG} in the S/H amplifier can be measured through the output voltage change ΔV_{OUT} after an observation time ΔT as

$$I_{LKG} = \frac{\Delta V_{OUT} C_{HOLD}}{\Delta T} \tag{5.23}$$

In all three circuits, the voltage change was recorded using an oscilloscope over time (Figure 5.17) and the slope $\Delta V_{OUT}/\Delta T$ was determined by linear regression. Right after the final sampling pulse, V_{IN} was brought down 1V to generate a stress across the switch. For this specific chip, the output voltages drop at 0.705μV/s and 12.74μV/s with TG- and BG-switch-enabled S/H amplifier with V_{IN} =1.65V, respectively.

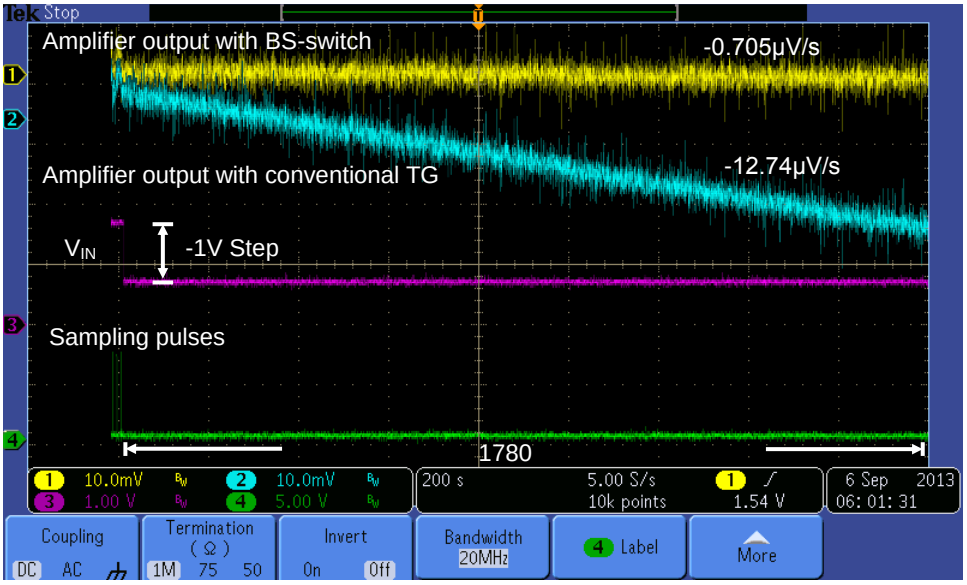


Figure 5.17: Measured output waveforms of S/H amplifiers (1: BS-switch, 2: conventional TG) together with input voltage (3) and sampling pulses (4).

To compare the BG-switch performance with conventional TG and prove its usefulness in the S/H amplifier, 63 chips were characterized at room temperature (22℃) with a sample voltage V_{IN} at mid-rail (1.65V). The histograms in Figure 5.18 show the I_{LKG} distribution over the sample set. The resulting current averages are 114±408aA (3σ) and -8.75±12.02aA (3σ) for the TG and BG-switch-enabled S/H amplifiers, respectively.

If averaging is done after taking absolute values of I_{LKG}, which is more meaningful, the BG-switch yields a 21dB improvement in device leakage over TG (12.02aA vs. 135.59aA).

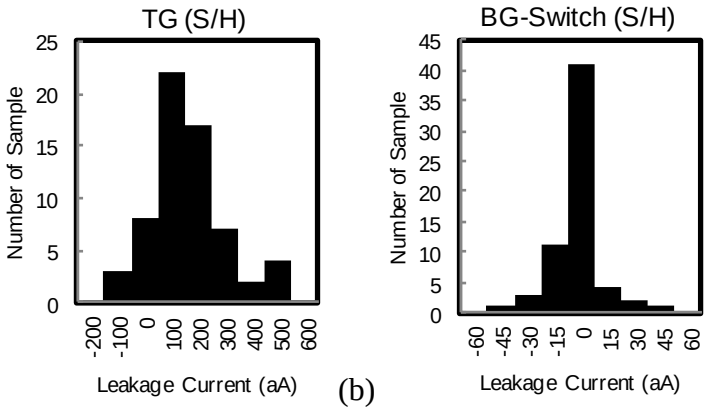


Figure 5.18: Leakage current distribution across 63 samples of S/H amplifiers (a) with TG (114±408aA (3σ)) and (b) with BG-Switch (-8.75±12.02aA (3σ)).

Since the S/H amplifier should not only operate at a single voltage point, we measured I_{LKG} of a chip with average performance at room temperature across an input voltage range from 0.3V to 3V considering the input/output voltage range of the on-chip buffer. A strong voltage dependency of I_{LKG} in the TG-enabled circuit was observed (Figure 5.19), which was further investigated in the time domain by sampling a $1.65\pm1.3V_{P\text{-}P}$ sinusoidal wave (Figure 5.20). This V_{IN} dependency is the result of changing voltage stress at the leakage sensitive node. To ensure the switch can operate in practical applications during the holding time, a +1V stress is applied to V_{IN} when V_{HOLD} is below 1.65V, while a -1V stress is applied when the V_{HOLD} is above 1.65V.

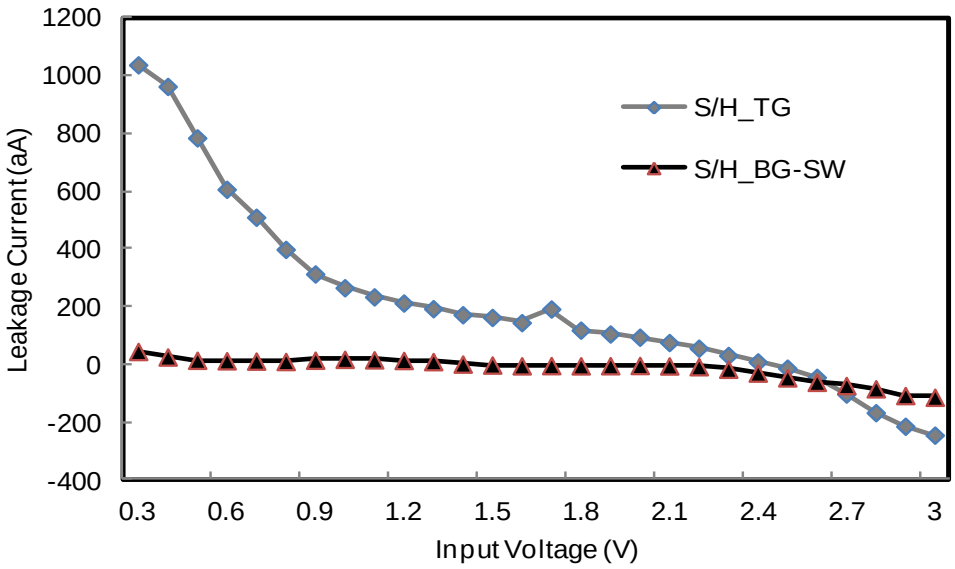


Figure 5.19: Switch leakage current in S/H amplifiers as a function of the input voltage. Switches with average leakage current based on the statistical results in Figure 5.18 were chosen for this measurement.

In some applications, such as bio-implantable chips, the circuit temperature dependency is not a big concern. However, many applications require stable circuit performance across a wide temperature range. Thus, the circuit leakage current was measured from -40℃ to 120℃ (Figure 5.21), indicating a reduced leakage of the BG-switch-enabled circuit up to 100℃. This is not a surprising result, because even a ~mV buffer offset, which can forward bias either the NMOS or the PMOS body diode, can generate a large diode current at high temperature.

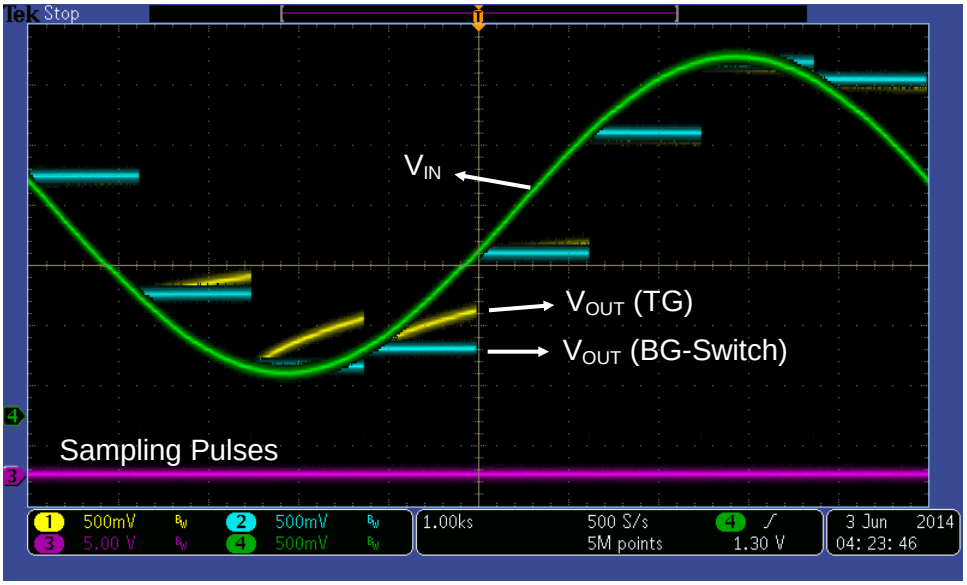


Figure 5.20: Time-domain view of voltage dependency of leakage current in TG and BG-switch. V_{IN} is a sinusoidal wave of $\pm 1.3V_{P\text{-}P}$ biased at 1.65V.

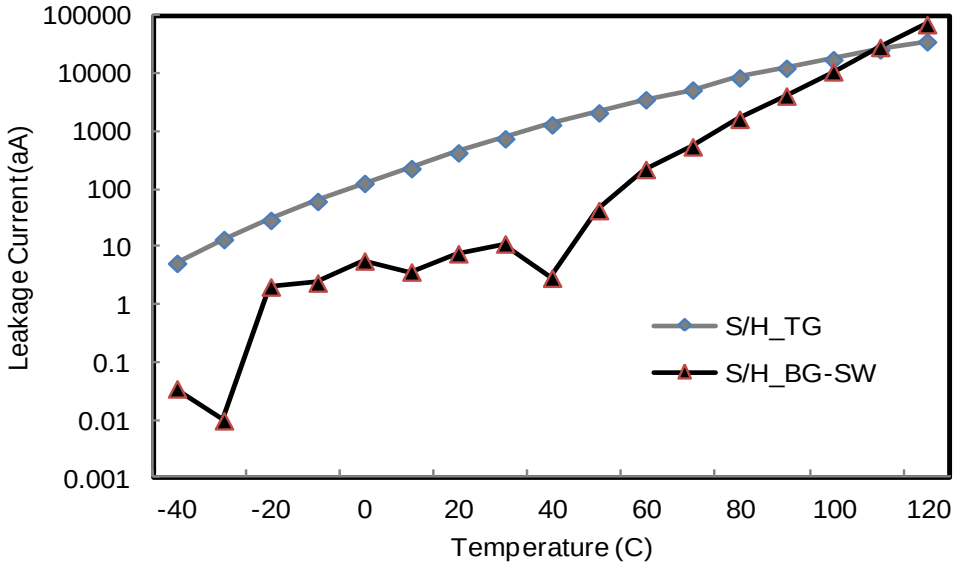


Figure 5.21: Switch leakage current in S/H amplifiers as a function of temperature. Switches with average leakage current based on the statistical results in Figure 5.18 were chosen for this measurement.

5.4.2 Switched-Capacitor Amplifier

The implementation of the BG-switch in a SC inverting amplifier is shown in Figure 5.22. The inverting input of the operational amplifier (OPA) is the leakage sensitive node, where the leakage current flows into the BG-switch connected across C_{FB}. To drive the BG-switch body terminal, we can simply use the on-chip V_{REF} instead of a buffer because the leakage sensitive node is always kept around V_{REF} through the negative feedback. The inverting amplifier in this work is designed to provide a 40dB gain to the signal difference between V_{IN} and V_{REF}. C_{FB} and C_{IN} are chosen to be 119.9fF and 11.99pF, respectively.

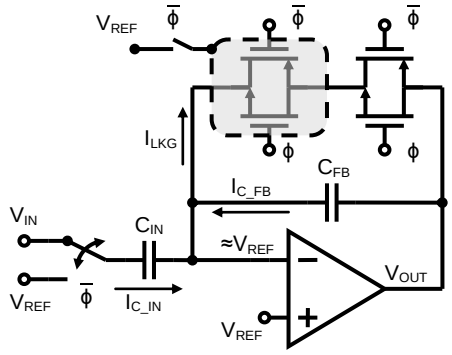


Figure 5.22: Schematic of SC amplifier employing BG-switch. I_{C_FB} and I_{C_IN} denote switch leakages flowing through C_{HOLD} and C_{IN}, respectively. I_{LKG} is the total leakage current through the switch.

The leakage current in the SC amplifier is the sum of I_{C_FB} and I_{C_IN} (Figure 5.22) from two different capacitors C_{FB} and C_{IN}, respectively. It can be shown that the ratio of I_{C_FB} to I_{C_IN} is given by

$$\left|\frac{I_{C\_FB}}{I_{C\_IN}}\right| = A\frac{C_{FB}}{C_{IN}} \tag{5.24}$$

where A is the open-loop gain of the OPA. This means the switch leakage current I_{LKG} is dominated by I_{C_FB}, and hence we can follow the same approach in (5.23) to have

$$I_{LKG} \cong I_{C\_FB} = \frac{\Delta V_{OUT} C_{FB}}{\Delta T} \tag{5.25}$$

The output waveforms of SC amplifiers employing TG and BS-switch are shown in Figure 5.23. After a 10ms sampling time, the amplifiers hold voltage for 100 seconds. For this specific chip, the output voltages drop at 177μV/s and 6.59mV/s with TG- and BG-switch-enabled SC amplifier with V_{IN} = -5mV, respectively.

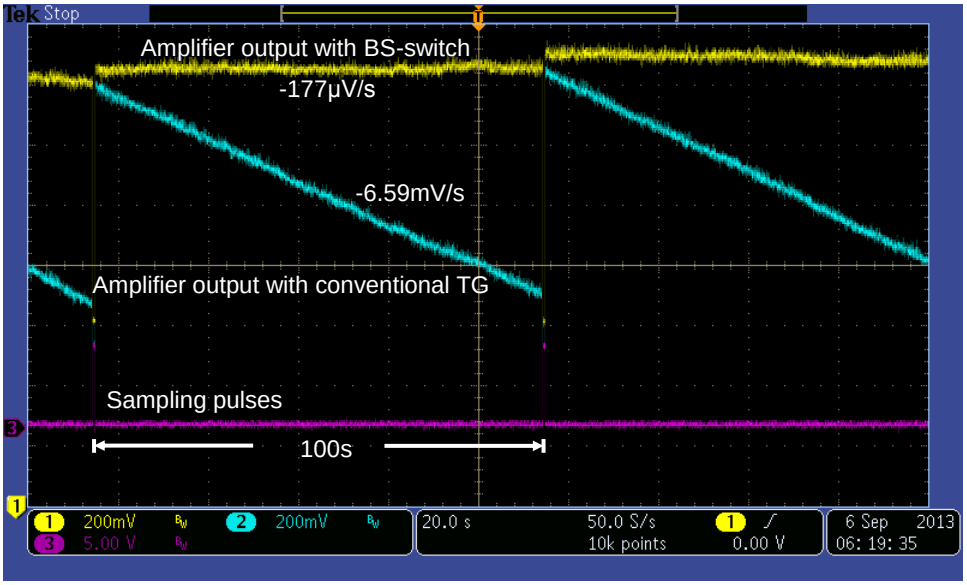


Figure 5.23: Measured output waveforms of inverting amplifiers (1: BS-switch, 2: conventional TG) together with sampling pulses (3) for a -5mV DC input voltage.

Again, 63 chips were characterized at room temperature and at -10mV DC input signal (Figure 5.24). The average leakage current in TG and BG-switch-enabled SC circuits were analyzed to be -1.376±3.42fA (3σ) and 33.43±178.9aA (3σ), respectively. The values are expected to be different from the S/H amplifier because the voltage stress at

the leakage sensitive node is now at an on-chip V_{REF} (~700mV) instead of 1.65V mid-rail. Considering again the averages of absolute I_{LKG} values, the BG-switch-enabled circuits show a 28dB improvement over the circuits with TG (1.368fA vs. 54.52aA).

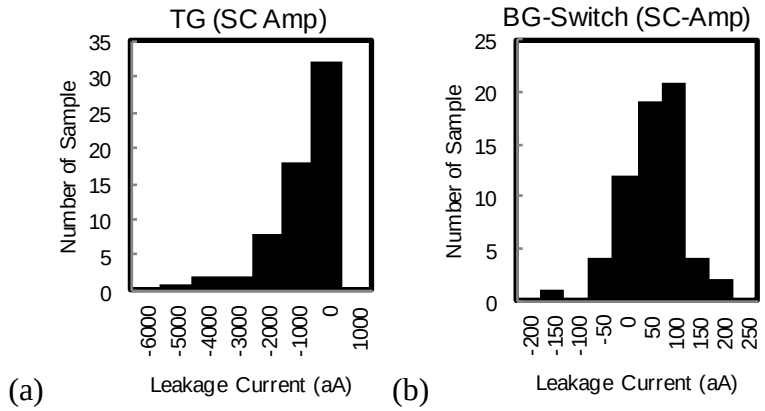


Figure 5.24: Leakage current distribution across 63 samples SC amplifiers (a) with TG (-1.376±3.42fA (3σ)) and (b) with BG-switch (33.43±178.9aA (3σ)).

Similar to the S/H amplifier, a measurement of I_{LKG} versus an input signal range from -20mV to 0V was taken with an average performance chip at room temperature (Figure 5.25). As expected, I_{LKG} does not show a strong dependency on V_{IN} since the voltage at the leakage sensitive node is always kept around V_{REF}. A measurement from -40℃ to 120℃ was also conducted using an average performance chip (Figure 5.26). The BG-switch-enabled SC circuit shows smaller I_{LKG} up to 110℃; similar to the S/H amplifier, forward biasing of the body diode reduces the performance at higher temperatures.

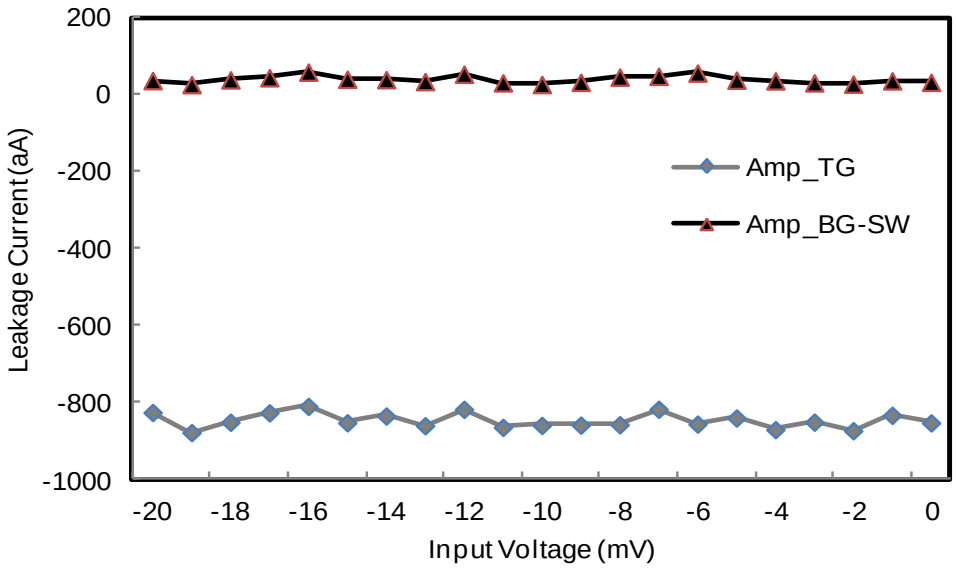


Figure 5.25: Switch leakage current in SC amplifiers as a function of the input signal. Switches with average leakage current based on the statistical results in Figure 5.24 were chosen for this measurement.

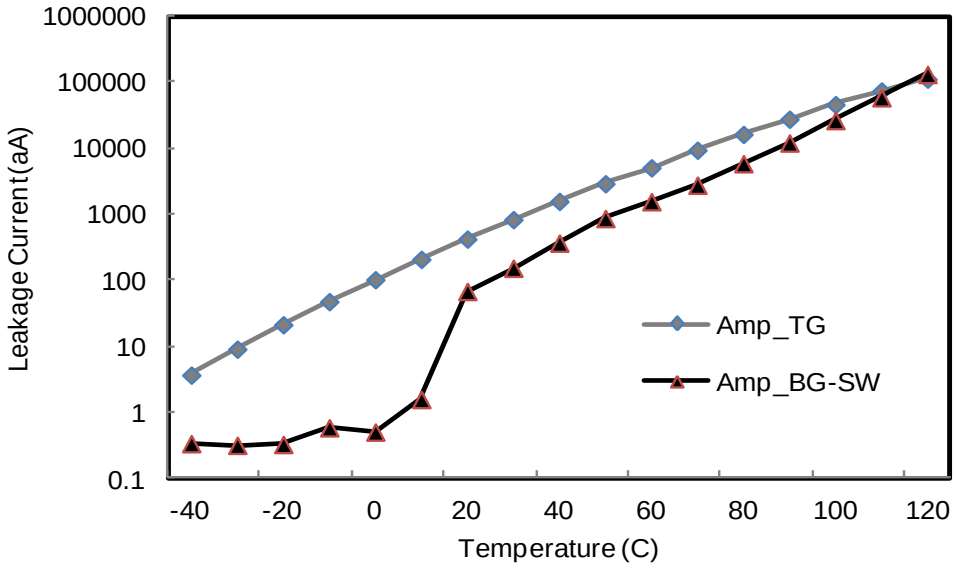


Figure 5.26: Switch leakage current in SC amplifier as a function of temperature. Switches with average leakage current based on the statistical results in Figure 5.24 were chosen for this measurement.

5.4.3 High-Voltage Switch

To show how the BG-switch technique can be applied to a DEMOS, we demonstrate a resettable high-voltage capacitor charger in Figure 5.27. C_{HOLD} is an off-chip capacitor holding voltage values determined by the number of switching cycles of a Dickson charge pump. A DEMOS is connected to C_{HOLD} to allow resetting and programming a time-varying V_{HOLD}. It has a large n-well diffusion drain, and it also sustains high voltage stress, which implies that large leakage currents could appear in the off state. When the BG-switch is applied, the body of the guarded DEMOS requires a bias close to V_{HOLD}. We can take advantage of the charge pump and place C_{BUF} to make a pseudo buffer. Usually, the small C_{BUF} is charged faster than C_{HOLD} and the excessive C_{BUF} voltage above V_{HOLD} will be discharged into C_{HOLD} through the parasitic diode in the BG-switch. In the reset period, C_{BUF} and C_{HOLD} will be discharged simultaneously to ground, and therefore, a body switch is unnecessary.

This high-voltage BG-switch technique is only applicable when both n- and p-buried layers are available in the process to build an isolated DEMOS. With a non-buffered D_O and a leaky C_{BUF} buffer, C_{BUF} should be reasonably large and D_O should be small to maintain a low reverse bias current, which is feasible in a low-speed application. D_O has an anode area of 5μm × 5μm. C_P and C_{BUF} are 2pF and 9.71pF, respectively.

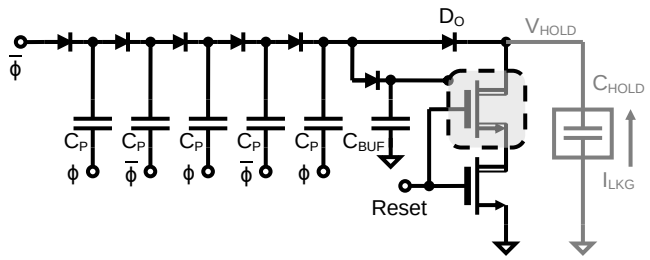


Figure 5.27: Schematic of resettable high-voltage capacitor charger employing DEMOS BG-switch. I_{LKG} denotes total leakages flowing through C_{HOLD} into BG-switch and D_O. Light gray part is outside the chip.

The leakage current of the charger circuit in Figure 5.27 can be measured through the drop rate of V_{HOLD}. However, the high voltage V_{HOLD} makes an on-chip buffer unavailable. Hence, an ultra-low input bias current (I_{IB}) off-chip buffer was used. Besides buffer I_{IB}, the external capacitor, printed-circuit board, chip carrier, package socket, and moisture contribute substantial leakage currents in sub-picoampere region. Consequently, the leakage measurement is split into two steps: 1. Measure both I_{LKG} and off-chip leakage currents. 2. Measure only the off-chip leakage currents and subtract this value from the total leakage in the first step. During the measurement, we found that off-chip leakage dominates the total leakage current. The recorded output waveforms of off-chip buffers are shown in Figure 5.28. Note that they are total leakages including both on-chip and off-chip leakages. Because the waveforms are nonlinear, only the first 0.5V drop was analyzed. For this specific chip, the output voltages drop at 1.056mV/s and 0.702mV/s with TG- and BG-switch-enabled SC amplifier with $V_{HOLD} \approx 10V$, respectively.

The two-step approach works decently for measurements carried out at room temperature; however, significant errors may occur when measuring performance at different temperature. There are multiple reasons involved. First, temperature causes par-

tially permanent variations in off-chip leakage. Taking the stabilization time of environment control chamber into account, the waiting time between the first and the second measurement steps may exceed 30 minutes. Permanent leakage changes during this period ultimately results in an error. Second, the humidity (and ice) at the surface of PCB strongly affects the off-chip leakage. Opening environment chamber and removing (or reinstalling) chip to exchange between step one and two at different temperature significant varies the humidity inside the chamber. Because the permanent variation of off-chip leakage exceeds the on-chip leakage, leakage versus temperature was not recorded.

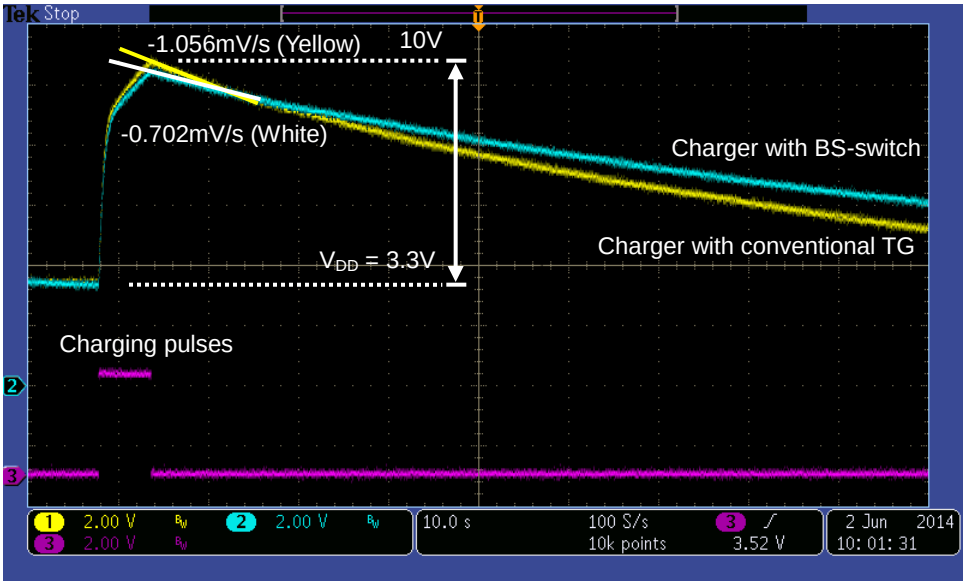


Figure 5.28: Measured output waveforms of resettable charge pump (1: conventional TG, 2: BS-switch) together with charging pulses (3) at ~10V output. Measurement was taken when both on-chip and off-chip leakages exist.

63 chips were characterized at room temperature and V_{HOLD} = 10V. The performance distributions are shown in Figure 5.29 with respective leakage current of -386.9±421.8fA (3σ) and -53.71fA±100.1fA (3σ) for the TG and BG-switch-enabled cir-

cuits (17dB improvement) under the restriction of negative values. I_{LKG} versus V_{HOLD} results shown in Figure 5.30 suggest that the residual I_{LKG} is limited around 100fA by the D_O reverse-bias current and the mismatch between base guarding voltage and V_{HOLD}.

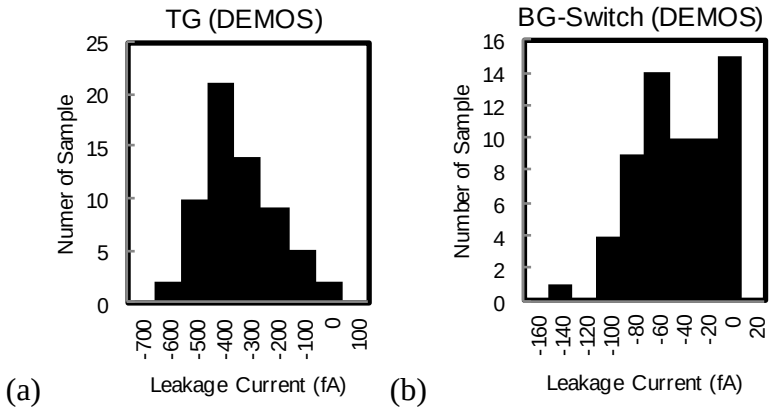


Figure 5.29: Leakage current distribution across 63 samples of resettable high-voltage capacitor chargers (a) with normal DENMOS (-386.9±421.8fA (3σ)) and (b) with BG-Switch (-53.71fA±100.1fA (3σ)).

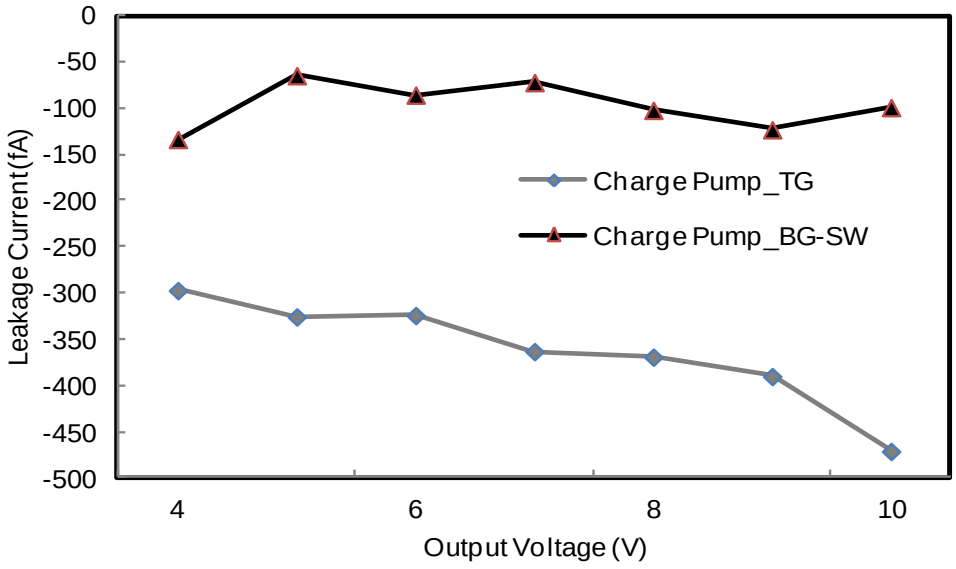


Figure 5.30: Switch leakage current in resettable high-voltage capacitor chargers as a function of V_{HOLD}. Switches with average leakage current based on the results in Figure 5.29 were chosen for measurement.

5.5 Full-System Characterization

The ChemFET interface circuit was fabricated with 0.35µm BiCMOS process and a microscopic picture of die is shown in Figure 5.31. The die occupies a 3.6mm×1.8mm area including all bonding pads. System characterization contains three parts. The first part is to verify the system functionality by measuring waveforms at V_D, V_G, S/H_{IN}, and S/H_{OUT} nodes. Next, an IGZO TFT was tested in constant current mode and an I_{DS}-V_{GS} relation was recorded by varying I_{DS}. Finally, measurement results for the boost converter efficiency versus V_C and t_{PL} were analyzed.

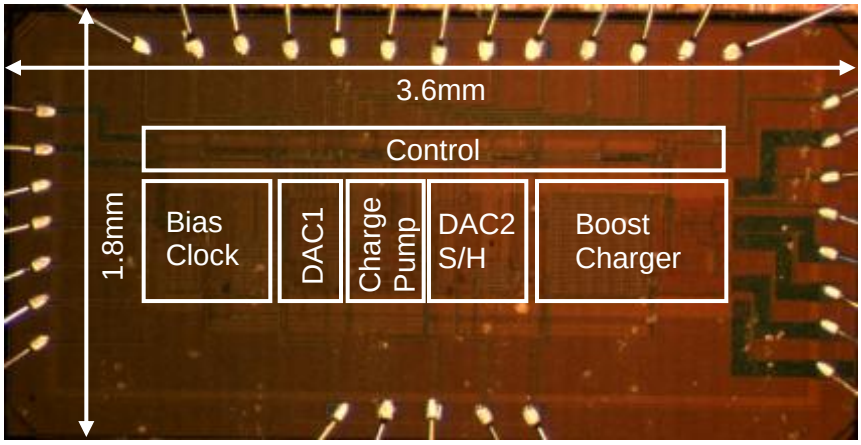


Figure 5.31: Microscope picture of ChemFET interface system. Total die area including all pads is 3.6mm×1.8mm.

The ChemFET interface output waveforms are shown in Figure 5.32 to Figure 5.34. Figure 5.32 demonstrates the waveforms of a complete measurement cycle; Figure 5.33 and Figure 5.34 are time-scale zooms into the beginning of charging and discharging periods. The measurements were taken in constant current mode close to the maximum circuit capability (V_{DS} = 13V, V_{GS} = 6.44V, and I_{DS} = 12.7µA) with an IGZO TFT as de-

vice under test. Each measurement node is buffered with an off-chip unity-gain buffer to avoid probe loading and leakage, while the connections between the interface and the TFT are not buffered.

In Figure 5.32, it can be seen that V_{DS} is charged to the target value of 13V (V_D = 16.3V above ground) much faster than V_{GS} to its target value of 6.44V (V_G = 9.74V above ground). As discussed earlier, the source terminal is biased at V_{DD} = 3.3V. A 1V V_{DS} drop after finishing charging C_{EG} is observed because of leakages and the slow recovery of the body diode in the current mirror. At the end of V_{GS} charging period, the switch controlling the discharge through the ChemFET (SW_{DC}) is closed for 2ms and the voltage across C_{EG} drops by about 7.7V. The voltage V_{S/H_IN} generated by the mirrored I_{DS} across an exchangeable resistor R_L at S/H_{IN} is given by the following relation,

$$V_{S/H\_IN} = \frac{1}{10} I_{DS} R_L \tag{5.26}$$

With I_{DS} = 12.7μA and R_L = 270kΩ, the sampled-and-hold amplifier holds the output voltage at 0.34V steadily for a whole measurement period. A small pulse at the input of the S/H amplifier which also has a 0.34V height can be seen close to the discharge edge.

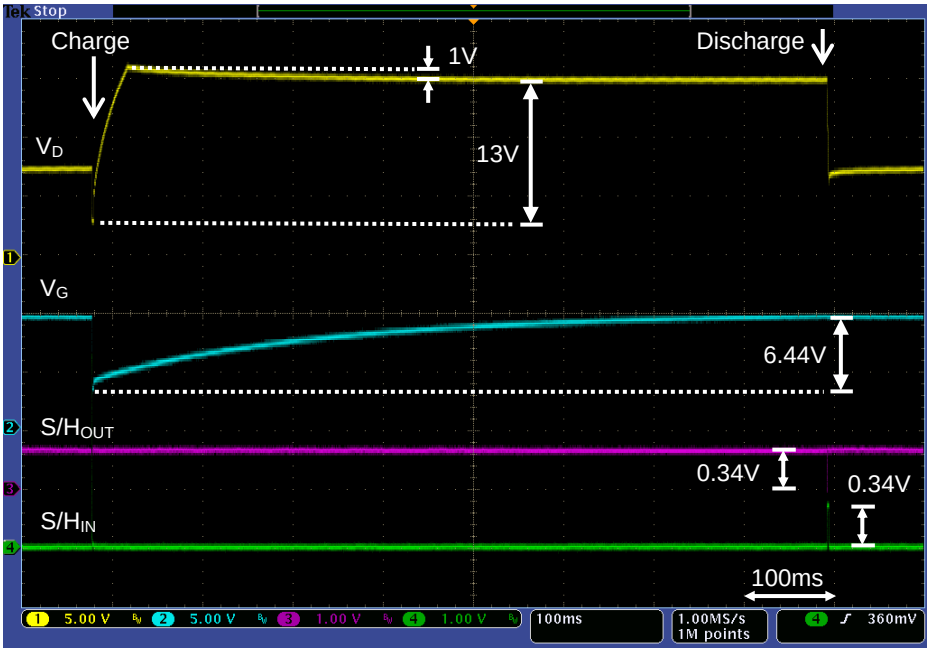


Figure 5.32: Oscilloscope waveforms of ChemFET interface system at V_D (1), V_G (2), S/H_{OUT} (3), and S/H_{IN} (4) nodes with I_{DS} = 12.7μA and targeted V_{DS} and V_{GS} at 13V and 6.44V, respectively.

The close-up of the beginning of the charging period (Figure 5.33) clearly shows the discrete charging steps for both V_G and V_D. Right before the charging period, both DC-DC converter outputs are rapidly discharged (reset) to V_{DD} for 2ms to ensure that every measurement cycle experiences the same charging waveforms. Parasitic signals stemming from the reset can be seen in S/H_{OUT} and S/H_{IN}. During the discharge phase (Figure 5.34), V_D decreases linearly with time (indicating a constant I_{DS}) and a signal at the S/H_{IN} node resulting from the mirrored I_{DS} is clearly seen during the discharge period. The voltage at the S/H_{OUT} node drops to zero and then slews to the S/H_{IN} voltage because of the delay of pulse at S/H_{IN} node. The S/H amplifier always begins holding the signal 1ms after the start of the discharge, which is in the middle of the S/H_{IN} pulse.

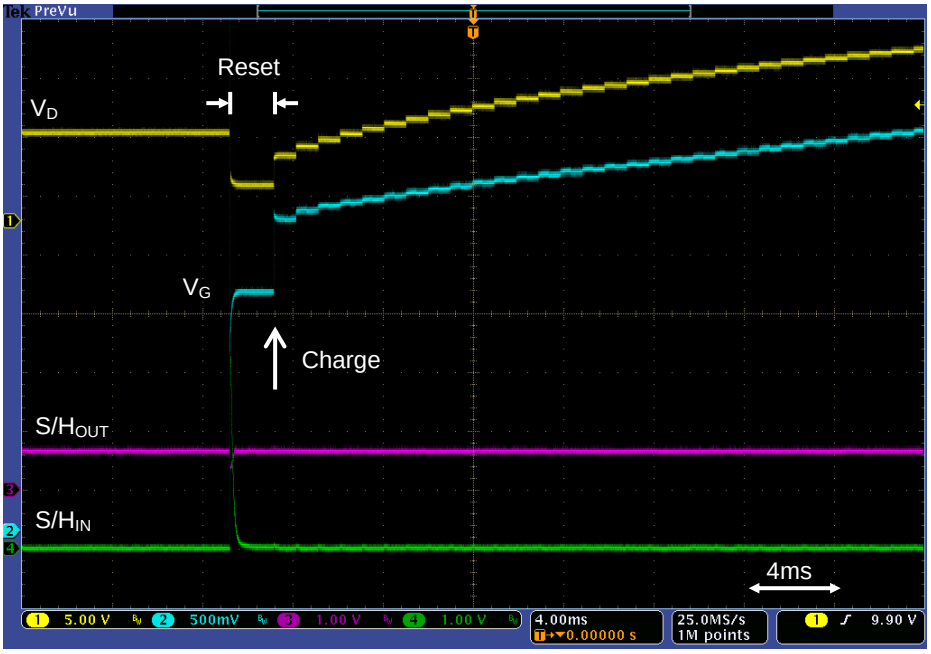


Figure 5.33: Time-expanded view of the waveforms at the beginning of the ChemFET interface charging period at V_D (1), V_G (2), S/H_{OUT} (3), and S/H_{IN} (4) nodes.

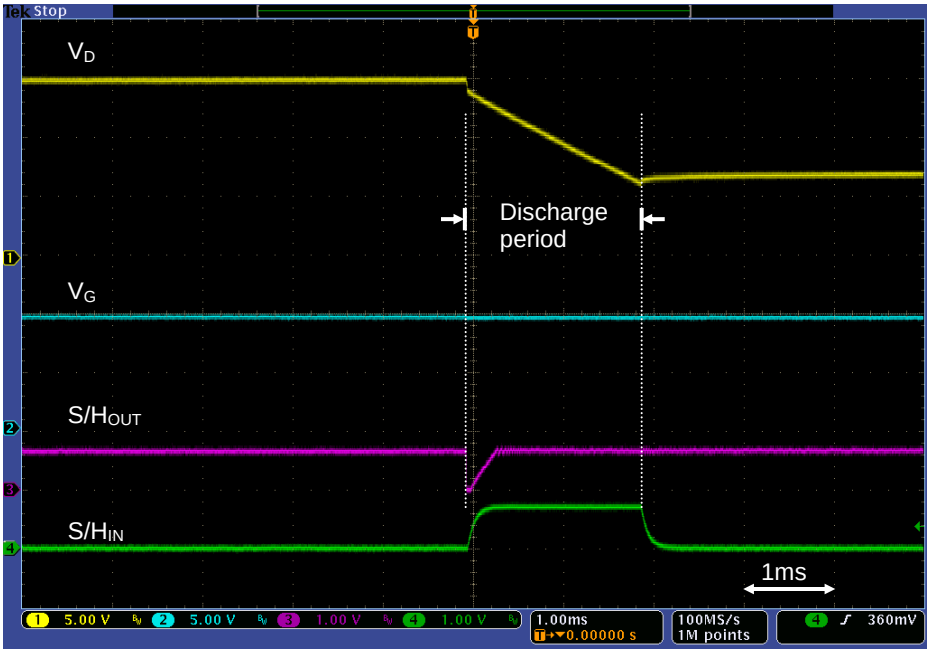


Figure 5.34: Time-expanded view of the waveforms at the beginning of the ChemFET interface discharging period at V_D (1), V_G (2), S/H_{OUT} (3), and S/H_{IN} (4) nodes.

A comparison of the I_{DS}-V_{GS} relations recorded with the proposed interface (solid line with square markers) and with a Keithley 2636A sourcemeter (dashed line) is shown in Figure 5.35. Above ~0.1μA, the I_{DS}-V_{GS} characteristic measured by the interface circuit follows the one measured with the reference instrument well with an approximately 20% shift in current level. Both measurements were taken after 3 minutes of stabilization time. However, the unique measurement approach employed by the proposed interface circuit results in a different bias stress compared to the sourcemeter measurement. In case of the sourcemeter, a continuous voltage bias is applied and I_{DS} is measured, while the developed interface biases and supplies I_{DS} discontinuously, relieving bias stress. It is believed that this reduced bias stress yields the larger currents measured with the interface circuit. At small current levels, a significant deviation in I_{DS} can be seen in the logarithmic scale. As V_G is tied to V_{DD} (3.3V), the measured V_S at low current level approaches V_{DD} and, thus, the minimum V_{GS} can be measured is limited by the input common mode range of the on-chip S/H amplifier, clamping V_{GS} around 0.4V.

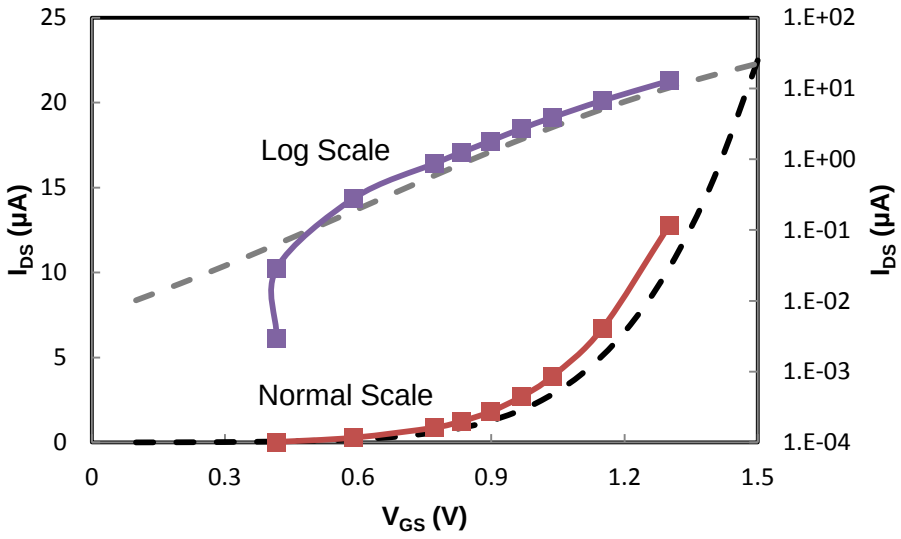


Figure 5.35: Comparison of TFT I_{DS}-V_{GS} curves measured with the developed interface circuit (solid line and rectangle) and a Keithley 2636A sourcemeter (dashed lines). The drain current is shown in both linear and logarithmic scales.

Finally, efficiency measurements of the boost capacitor charger as a function of V_C and t_{PL} have been made and are presented in a 3D plot (Figure 5.36). The measurements were carried out with a function generator (Agilent 33220A) and an oscilloscope (Tektronix TDS2022C). The function generator outputs a finite number of pulses with 100-1000ns pulsewidth to drive the charger to match the targeted V_C. Since the energy invested into the inductor in the energizing phase is the same, the efficiency is easily calculated by dividing the energy in the capacitor by the total energy investment. The best efficiency (blue ridgeline in Figure 5.36) is found for pulsewidth t_{PL} around 300-400ns. Compare to the simulation results in Figure 5.11, the overall efficiency surface is shifted to lower efficiency values as the simulation did not consider post-layout and off-chip parasitic capacitances and leakages, which can further degrade the efficiency. However, the overall characteristic is very similar and the simulation very well predicts the optimal

pulsewidth window between 300-400ns.

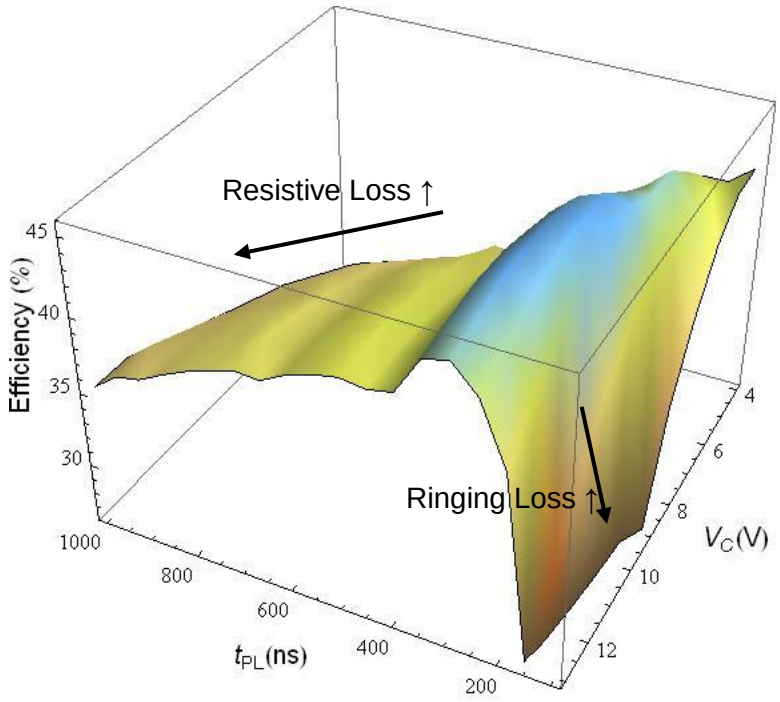


Figure 5.36: Measured boost capacitor charger efficiency as a function of t_{PL} and V_C.

Last but not least, the measured interface performance is compared with the targeted specifications in Table 5.3. Thereby, all measurements were done with external component values listed in Table 5.2. The power consumption was measured with Keithley 4687A picoammeter at maximum current and voltage ratings. Noise measurements were performed by recording signals at the S/H amplifier output with a LabView DAQ card for 5 minutes and calculating the standard deviation. The maximum achievable V_{GS} and V_{DS} values mostly do not meet the target specifications. The reasons are manifold: for the Dickson charge pump, the efficiency is reduced by the reverse-bias p-n junction leakage currents in the diode chain, which are not easily determined by simulation. Additionally, both converters have one off-chip feedback capacitor for trimming purposes.

Such off-chip components incur extra leakages and parasitic capacitances, which ultimately stop the charging process before reaching the target voltages.

Table 5.3: Comparison of measured ChemFET interface specifications compared to target specifications.

	Specifications	**Fabricated Circuit**
Power	<100μW	≤2.02μW
Readout Rate	~1Hz	1Hz
I_{DS}	Up to 10μA	≤15μA
V_{GS}	Up to 10V	Constant voltage mode: ≤6.44V Constant current mode: ≤9.74V
V_{DS}	Up to 15V	Constant voltage mode: ≤13V Constant current mode: ≤16.3V
Noise Level	ΔI_{DS} = 1% ΔV_T = 10mV	I_{DS} = 0.0476μA $_{RMS}$ (at 10μA) $V_T = 0.503mV_{RMS}$
Special Issues	Bias stress	Discontinuous measurement

CHAPTER 6

GAS-PHASE CHEMICAL SENSING MEASUREMENTS

The ultimate goal of this thesis is to perform chemical measurements by interfacing different chemical sensors with the proposed interface circuits. While the microfabricated sensors introduced in Chapter 3 were used, some measurements were also taken using commercial sensors to serve as reliable references. Chapter 6 begins with a brief introduction of the customized gas setup used for sensor testing. Then, chemical measurements with chemoresistors, chemocapacitors, and ChemFETs are subsequently highlighted.

6.1 Measurement Setup

A custom-made gas mixing system (see schematic in Figure 6.1) is used for sensor testing. The incoming carrier gas, either nitrogen or synthetic air, is split into three gas streams, with each one being individually controlled and monitored by a mass flow controller (MFC). At the beginning of the measurement and during the purge time, the reference stream (L3) flushes the test chamber with pure carrier gas. A gas stream loaded with the desired volatile organic compound (VOC) at its (temperature-dependent) saturation vapor pressure is generated by feeding carrier gas through a (temperature-controlled) bubbler containing analyte-soaked quartz sand (L1). The VOC-loaded gas stream is further diluted by a secondary carrier gas stream (L2) before flowing across the sensor mounted in the measurement chamber. The analyte concentration can be calculated from the saturation vapor pressure of the analyte at the bubbler temperature and the mixing ra-

tio between lines L1 and L2.

Rapid switching between reference flow and the diluted analyte mixture is realized with a pneumatically actuated 4-way valve. A flow meter is appended at the end of measurement chamber to continuously monitor the total flow rate. In this work, the total flow rate was kept at 80ml/min and synthetic air (80% N_2 and 20% O_2) was used as a carrier gas to simulate real atmospheric conditions. The gas setup is controlled by a dedicated LabView program through a DAQ card. A secondary DAQ card is installed in the same desktop for acquiring digital bit streams from the passive impedimetric sensor interface and analog signals from the ChemFET interface.

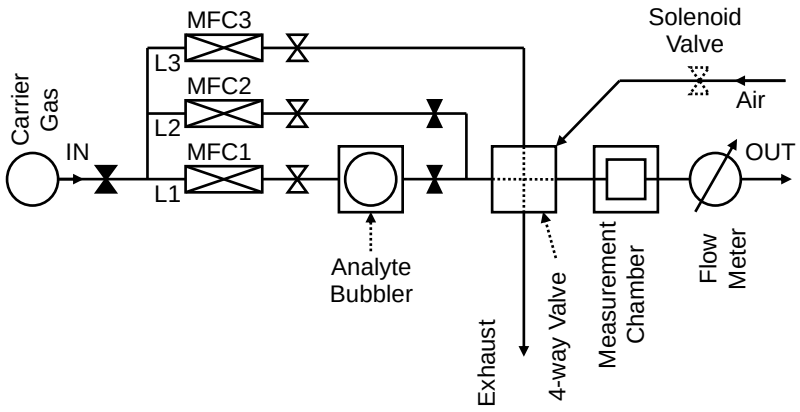


Figure 6.1: Schematic of gas testing set-up with analyte (L1), diluting (L2), and reference (L3) gas lines.

6.2 Chemoresistor Measurements

Chemical measurements using the passive impedimetric sensor interface were first taken using a commercial metal-oxide (MOx) alcohol sensor (TGS2620, Figaro Engineering Inc.). Following the suggestions given in the datasheet, the TGS2620 was pre-

conditioned in the gas setup (i.e., applying a heater voltage of 5V, corresponding to 160mW power consumption) under synthetic air flow for more than a day until the base-line resistance stabilized at ~120kΩ. Both DC (Figure 6.2) and Pseudo-AC (Figure 6.3) measurements were performed and almost no visible difference is found in the shape of the sensor response, implying that MOx sensors do not suffer from polarization effects. The resistance values shown in the graph have been calibrated based on equation (4.23). For this specific chip, M_R, G_{Err}, and R_{nom} are calculated to be 1033.25, -8.12059×10^{-11}, and 14.69057, respectively.

In both measurements, the MOx sensor was exposed to four different concentrations of ethanol from 750 to 3000ppm at room temperature (22℃). Each 30-minute analyte exposure cycle is followed by refreshing the sensor with synthetic air for another 30 minutes. As expected, the decrease in resistance is strong (>2 decades) and highly nonlinear. The range of resistance variation within the 8.5 hours measurement can be accommodated by the low-resistance sub-range of the interface circuit. Looking at Figures 6.2 and 6.3, the time constants associated with analyte desorption appear much longer than the adsorption time constants. This difference in time constants is largely the result of the nonlinear sensing behavior of MOx sensors (see Figure 6.4 or refer to [18]), which exhibit a higher sensitivity at lower analyte concentrations.

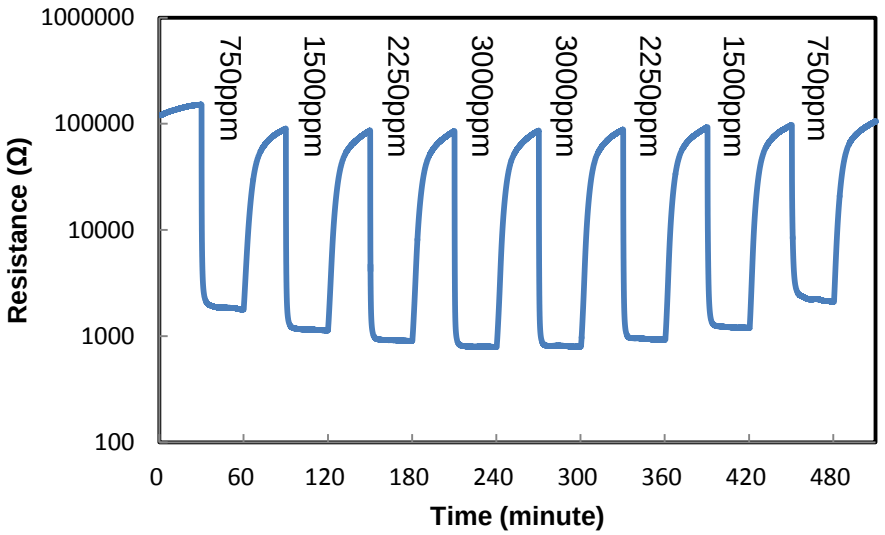


Figure 6.2: Resistance change of MOx sensor upon ethanol exposure with concentrations of 750, 1500, 2250, 3000, 3000, 2250, 1500, and 750ppm under continuous DC biasing. In-between each concentration step, the measurement chamber is flushed with synthetic air as reference gas for 30 minutes.

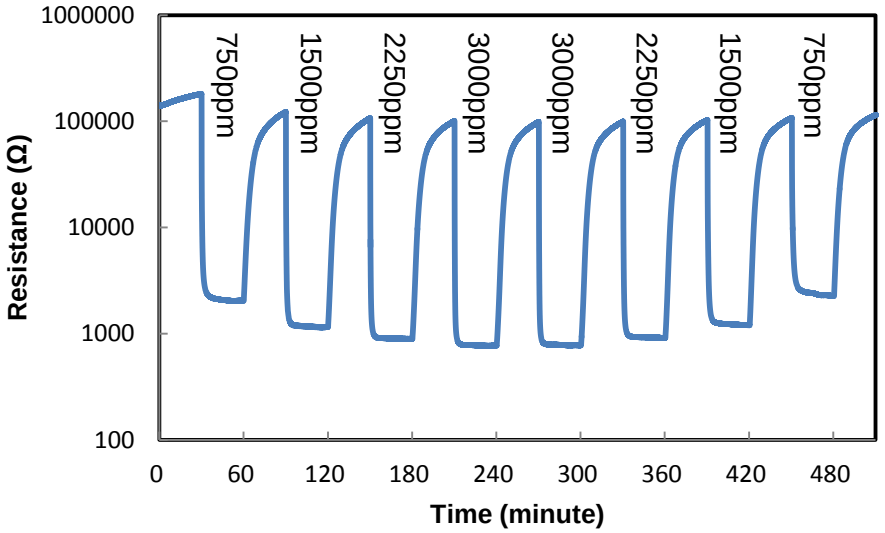


Figure 6.3: Resistance change of MOx sensor upon ethanol exposure with concentrations of 750, 1500, 2250, 3000, 3000, 2250, 1500, and 750ppm under pseudo-AC biasing. In-between each concentration step, the measurement chamber is flushed with synthetic air as reference gas for 30 minutes.

The response versus ethanol concentration of both DC and AC measurements are plotted and compared to datasheet values [18] in Figure 6.4. Since the process variation of baseline resistance is significant, plotting the change ratio with respect to baseline resistance is more meaningful than the absolute resistance values. As shown in Figure 6.2 and 6.3, no significant difference is found between DC and AC measurements; however, the chemical measurement shows about three times less in signal strength. The reason could be a combination of multiple differences in testing conditions and device variations. For instance, sensor temperature and MOx film quality could vary between different devices. Moreover, the accuracy of analyte concentration and the composition of carrier gas, especially the oxygen concentration and relative humidity, used during the measurement are important roles that affect both baseline resistance and responses.

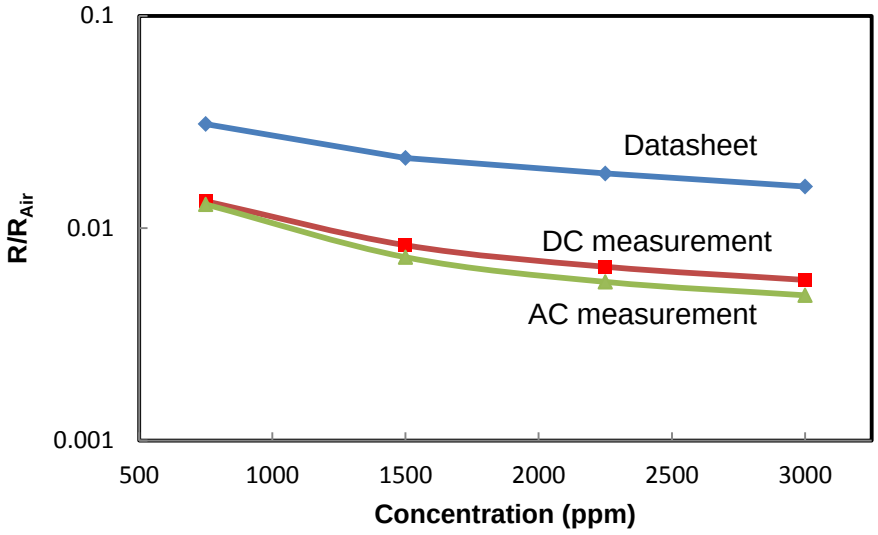


Figure 6.4: Sensor response as function of ethanol concentrations. R/R_{Air} denotes the response normalized to the sensor resistance in an ethanol-free environment. Measured chemical responses are extracted at 45, 105, 165, and 225 minutes in figures 6.2 and 6.3; R_{Air} is extracted at 15 minute.

Besides the commercial MOx sensor, a chemoresistor measurement was carried out with the multi-functional impedimetric sensor introduced in Chapter 3. To this end, a sensor with 6μm electrode pitch was drop-coated with PEDOT:PSS conducting polymer purchased from Sigma-Aldrich #560596 (2.8wt% dispersion in H_2O, low-conductivity grade). The PEDOT:PSS solution was diluted 20 times with de-ionized water before drop coating, resulting in a polymer film thickness of 1-2μm. To obtain a better sensing film quality, the coated sensor was placed in an environmental chamber at 10℃ to slow down the evaporation of the solvent (water) while drying polymer film. Low temperature results in a film with less cracks than the film prepared at high temperature.

The chemoresistor with PEDOT:PSS coating was exposed to the same ethanol concentrations (750-3000ppm) as the MOx sensor at room temperature (22℃) (Figure 6.5). After each 5-minute analyte exposure, the sensor was exposed to synthetic air for another 5 minutes. As performing DC measurements can degrade the film quality (Chapter 3), a pseudo-AC measurement in high-resistance mode was performed. The measurement result obtained with the interface IC is consistent with the results shown in Figure 3.5, in that the film resistance increases with increasing ethanol concentration. However, the resistance changes reported in Figure 6.5 are larger (30% compared to 5% change in Figure 3.5). The higher sensitivity may be caused by different film thicknesses and the temperature used for drying the polymer film, 10℃ and 50℃ for device used in Figure 6.5 and Figure 3.5, respectively.

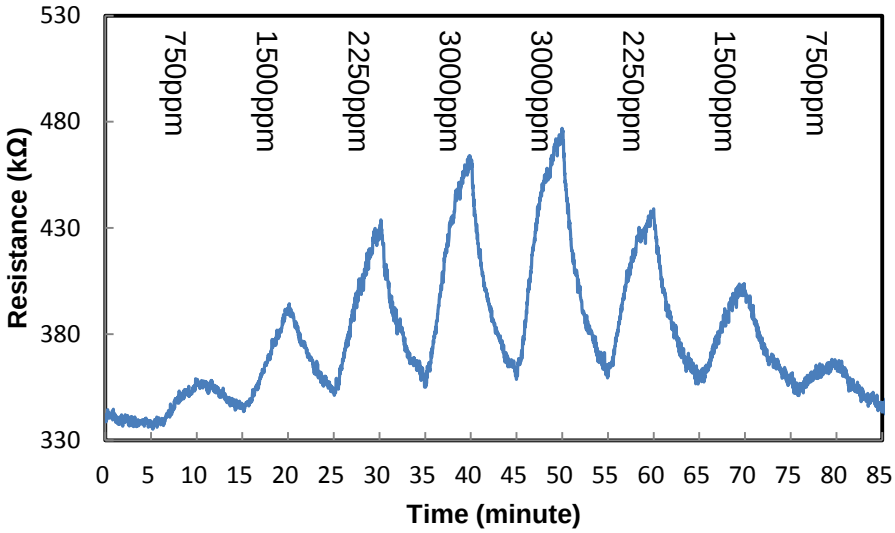


Figure 6.5: Resistance change of multi-functional sensor coated with PEDOT:PSS upon ethanol exposure with concentrations of 750, 1500, 2250, 3000, 3000, 2250, 1500, and 750ppm under pseudo-AC biasing. In-between each concentration step, the measurement chamber is flushed with synthetic air as reference gas for 5 minutes.

6.3 Chemocapacitor Measurement

To perform a chemocapacitor measurement, a multi-functional chemical sensor having a 3μm electrode pitch and a 2mm×2mm size was coated with the non-conducting polymer poly(epichlorohydrin) (PECH) and tested with the passive impedimetric sensor interface. To this end, a 1wt% PECH/chloroform solution was drop-coated on the sensor. The chemocapacitor was exposed to different concentrations of ethanol from 7500 to 30000ppm (Figure 6.6) and toluene from 4000 to 16000ppm (Figure 6.7) at room temperature (22℃). As expected, the exposure to ethanol (dielectric constant of 24.5) results in an increase in capacitance and the exposure to toluene results in a decrease in capacitance, considering that the dielectric constant of PECH (ε_r = 7-8) lies in between that of ethanol (ε_r = 24.3) and toluene (ε_r = 2.4). Compared to the chemocapacitors tested in Chapter 3 (coated by spray coating), the drop-coated polymer films are visually much

thicker and the analyte diffusion time constant is longer. Thus, 30 minutes analyte exposure and purge time were used in the measurement.

Figure 6.6 and Figure 6.7 show stronger responses to ethanol and weaker responses to toluene, compared to the sensor results discussed in Chapter 3 (Figure 3.4). In addition, the measurements presented in this chapter exhibit a stronger non-linearity, with the sensor sensitivity clearly increasing with increasing ethanol concentration (Figure 6.6) and decreasing with increasing toluene concentration (Figure 6.7). It is speculated that the difference in polymer thickness and the polymer deposition technique (drop vs. spray coating) may cause the different results. Generally, one would expect that a thinner film has its response dominated by the film swelling effect, with film swelling always causing a positive capacitance change, because air is displaced by analyte-loaded polymer. Thus, with decreasing film thickness, one would expect that the toluene sensitivity decreases while the ethanol sensitivity increases. The test results in Chapter 3 and Chapter 6 seem to show the opposite trend. However, the effect of polymer adhesion and the degree to which the polymer can fill the gaps between the electrodes are different when spray or drop coating is applied and the resulting impact on the measurement results is unclear. Furthermore, the swelling of the polymer causes different stresses acting on the substrate, resulting in a different stress-dielectric response (dielectrostriction) [138]. More measurements are needed to better understand the sensor response, which goes beyond the scope of this thesis focusing on interface circuits.

An additional difference between the measurement taken with the developed sensor interface and the initial measurements taken in Chapter 3 is the way the capacitance is measured. While the proposed interface probes the capacitance quasi-statically, the Ag-

ilent LCR meter used in Chapter 3 tests the capacitance at a frequency of 1kHz. Figure 6.8 shows the capacitance of the PECH-coated chemocapacitor as a function of measurement frequency. The result in Figure 6.8 shows a lower capacitance compared to Figures 6.6 and 6.7 because the chemocapacitor was measured without the long test leads connecting the package carrying chemocapacitor to the PCB.

It could also be speculated that the nonlinearity may be caused by the change in the integration time, and hence the frequency, of the interface circuit. However, the corresponding frequency change at the maximum response (30000ppm exposure) is only about 1Hz around 50Hz sampling rate. According to the frequency dependency measurement of the chemocapacitor (Figure 6.8), the change in capacitance due a 1Hz variation around 50Hz is only about 20fF.

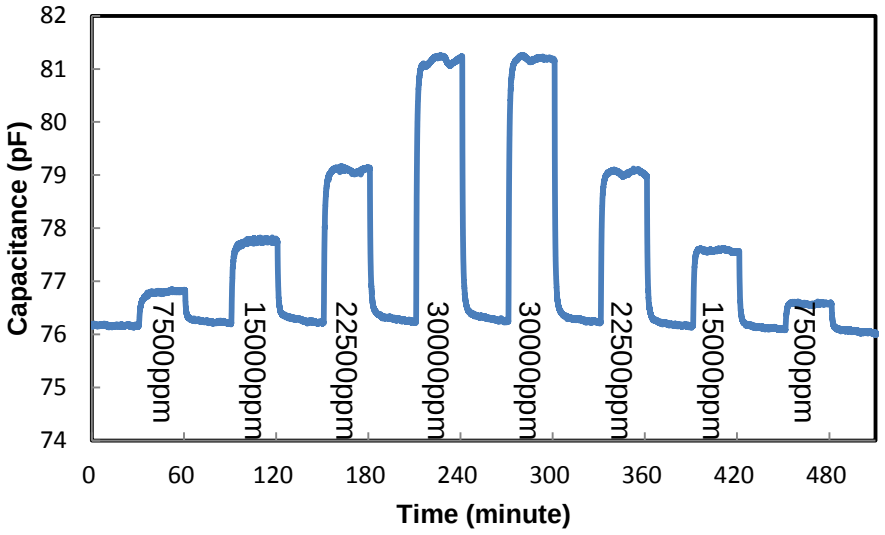


Figure 6.6: Capacitance change of multi-functional sensor coated with PECH upon ethanol exposure with concentrations of 7500, 15000, 22500, 30000, 30000, 22500, 15000, and 7500ppm. In-between each concentration step, the measurement chamber is flushed with synthetic air as reference gas for 30 minutes.

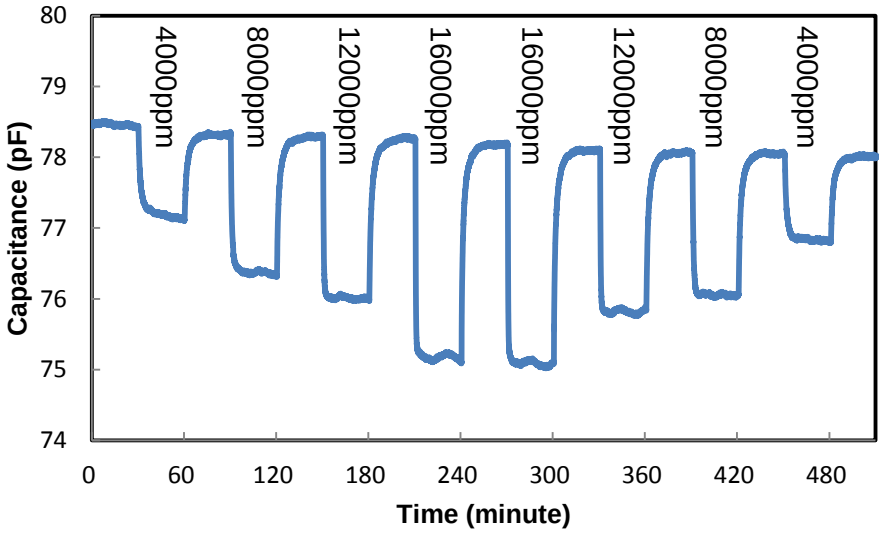


Figure 6.7: Capacitance change of multi-functional sensor coated with PECH upon toluene exposure with concentrations of 4000, 8000, 12000, 16000, 16000, 12000, 8000, and 4000ppm. In-between each concentration step, the measurement chamber is flushed with synthetic air as reference gas for 30 minutes.

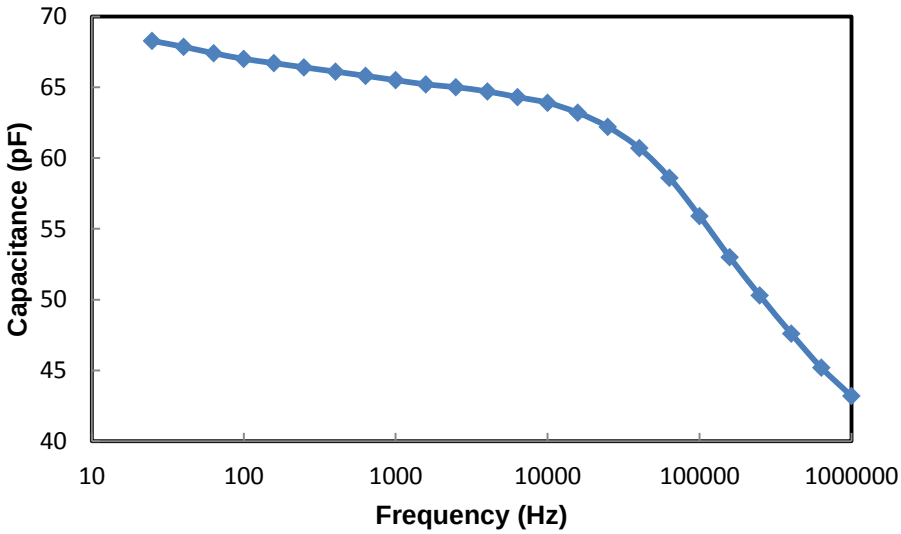


Figure 6.8: Measured capacitance of the PECH-coated chemocapacitor as a function of excitation signal frequency ($1V_{RMS}$) from 20 to 1MHz. Measurement data is taken with Agilent 4284A LCR meter.

6.4 Chemical Field-Effect Transistor (ChemFET) Measurement

Finally, a chemical measurement of a ChemFET connected to the developed ChemFET interface circuit was carried out with an uncoated and unpassivated IGZO TFT with 5μm channel length. The TFT was annealed on a hotplate at 300℃ for about 90 minutes to reduce current instability. However, we still experienced a ~250mV threshold voltage reduction during the initial 30-minute stabilization period. Hence, we decided to perform constant current measurements to avoid any subsequent readjustment of the bias voltages to maintain drain current in a reasonable range. The applied I_{DS}, V_G, and V_D are 1.24μA, 3.3V, and 16V, respectively.

Figure 6.9 shows the measured relative change of threshold voltage upon exposing to 7500 to 30000ppm of ethanol vapor with analyte exposure and purge times of 5 minutes at room temperature (22℃) In constant current mode, the gate is biased at 3.3V and, thus, measuring the change in source voltage is the same as measuring the change in threshold voltage. A -70μV per minute threshold voltage drift has been removed from the measurement data. Compared to the measurement with a bare TFT in Chapter 3, an increase in threshold voltage (Figure 6.9) when exposing to ethanol is in consistent with a decrease in drain current (Figure 3.9). Based on the characterization data in Figure 5.35, the threshold voltage and the gate-source voltage are calculated to be 0.914V and 1.17V, respectively. By applying (2.3), a ~12mV threshold voltage change upon responding to 30000ppm ethanol will induce a current change ~0.116μA. Comparing to the device measured in Figure 3.9, which is biased at 10μA in subthreshold region, the calculated result with (2.4) yields a ~4.7mV (~0.6μA grain current decrease) increase in threshold voltage when exposing to 25500ppm of ethanol. Hence, both measurements results in

threshold voltage change in the same order. The noisy signal in Figure 6.9 is largely due to the long test leads and electromagnetic interference (EMI) generated by the gas setup. It should also be note that the ChemFET interface is not optimized for noise performance.

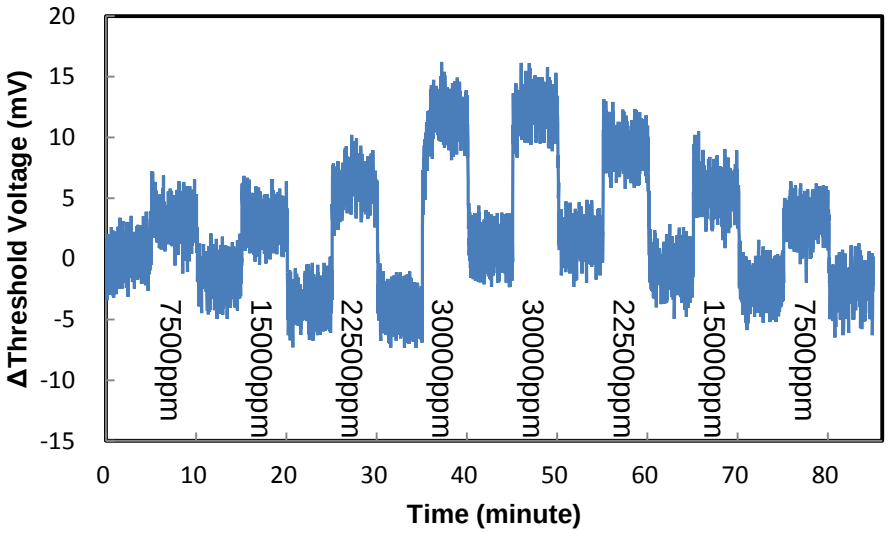


Figure 6.9: Relative threshold voltage change of IGZO TFT ChemFET upon ethanol exposure with concentrations of 7500, 15000, 22500, 30000, 30000, 22500, 15000, and 7500ppm. In-between each concentration step, the measurement chamber is flushed with synthetic air as reference gas for 5 minutes.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Major Results

This thesis presents two interface circuits for impedimetric chemical sensors: one for passive chemical sensors and the other for ChemFETs. Both interfaces were fabricated in 0.35μm BiCMOS technology and provide the same output data rate of 1Hz.

The interface for passive impedimetric sensors is reconfigurable for performing either resistance or capacitance measurements and provides a fully digital output with less than 81.8μW power consumption at V_{DD} = 2.5V. The interface features a 176dB resistance dynamic range (31.6Ω-200MΩ, <±0.8% nonlinearity, and >40dB SNR) realized with only two sub-ranges to minimize calibration efforts and a 102dB capacitance dynamic range (0.8-1000pF, <±0.2% nonlinearity, and >40dB SNR).

The ChemFET interface is a highly versatile system that can generate a wide range of bias voltages (V_G up to 9.74V and V_D up to 16.3V depending on the measurement modes) and perform either constant voltage or constant current mode measurement. At maximum rated output (V_G = 9.74V, V_D = 16.3V, and I_{DS} = 15μA), the interface consumes only 2.02μW at V_{DD} = 3.3V and provides analog readout noise levels of $0.0476\mu A_{RMS}$ at 10μA and $0.503mV_{RMS}$ for I_{DS} and V_T, respectively.

Besides attempting versatile system architectures, detailed noise and efficiency analysis were performed for the passive sensor interface and the ChemFET interface, respectively. The noise analysis suggests that different types of noise (correlated or uncorrelated) dominate the noise performance in different measurement ranges and, thus, noise

suppression techniques, such as chopper stabilization, correlated double sampling (CDS), and oversampling/averaging, are applied to adequate parts of the interface system. The efficiency analysis of the boost capacitor charger in the ChemFET interface concludes that applying a moderate pulsewidth (200-300ns) to drive the boost converter yields the best efficiencies for charging a capacitor.

Compared to interfaces described in the literature, the proposed interface for passive sensors achieves better versatility and wide dynamic range with less number of sub-ranges and power consumption. The proposed interface for ChemFETs achieves wider voltage supply range at very low power level.

In-house fabricated chemical sensors, including passive chemical sensors and ChemFETs, were interfaced with the developed circuits and gas-phase chemical measurements with the systems were demonstrated. The novel passive chemical sensor tested in this thesis employs a multi-functional design, which can be configured into either a chemoresistor or a chemocapacitor; the tested ChemFET employs a bottom-gate TFT structure to allow the semiconducting film to interact with the analytes.

7.2 Future Work

The focus of this thesis is on developing versatile and low-power interface circuits for impedimetric chemical sensors. While two particular designs have been successfully implemented, multiple issues have not been considered in the proposed interfaces. In case of the passive chemical sensor interface, temperature variations, both of the sensor or the circuit, have not yet been taken into account. Temperature instabilities can be accommodated by, e.g., adding additional temperature compensation circuits, recalibrating the

sensor impedance periodically, or modifying the system control for performing ratiometric or differential measurements. On the other hand, although the ChemFET interface is designed for generic ChemFETs (not only for ISFETs), it is essentially for generic n-channel ChemFETs, such as the intrinsically n-type IGZO films used in our TFTs. However, most ChemFETs found in the literature, especially organic TFT (OFET) ChemFETs, are p-type devices [38]. To accommodate p-type ChemFETs, the proposed interface may be modified to allow the charger to reconfigure into an inverting boost charger architecture to supply negative voltages. Furthermore, temperature compensation and digital output features were not implemented with the initial ChemFET interface. Finally, for even broader applicability, wireless communication functions may also be co-integrated with on-chip chemical sensors and associated interface circuits.

APPENDIX A

PROOF OF EQUVALRENT PSEUDO INDUCTOR CURRENT

Equation (5.10) is only based on the intuition of energy balancing and, thus, it requires a strict proof. Consequently, we derive (5.10) by means of solving an equivalent second-order differential equation of the system (Figure A.1), assuming that the series resistance is negligible. Applying Kirchhoff's circuit law,

$$V_C(t) + V_D + V_L(t) = 0 \tag{A.1}$$

$$C_{EG} L \frac{d^2 V_C(t)}{dt^2} + V_C(t) + V_D = 0 \tag{A.2}$$

The solution of (A.2) in the n-th cycle with $V_C(0) = V_{C,n-1}$ and $V_C'(0) = I_{L\_MAX}/C_{EG}$ yields,

$$V_C(t) = -V_D + \left(V_{C,n-1} + V_D\right)\cos\left(\frac{t}{\sqrt{LC_{EG}}}\right) + I_{L\_MAX}\sqrt{\frac{L}{C_{EG}}}\,\mathrm{Sin}\left(\frac{t}{\sqrt{LC_{EG}}}\right) \tag{A.3}$$

The inductor current in the n-th cycle is,

$$I_{L,n}(t) = C_{EG}\frac{dV_C(t)}{dt} = I_{L\_MAX}\cos\left(\frac{t}{\sqrt{LC_{EG}}}\right) - \sqrt{\frac{C_{EG}}{L}}\left(V_{C,n-1} + V_D\right)\sin\left(\frac{t}{\sqrt{LC_{EG}}}\right) \tag{A.4}$$

By expressing $I_{L,n}(t)$ in the form of $A\times\sin(\omega t+\theta)$ yields,

$$A = \sqrt{\frac{C_{EG}}{L}\left(V_{C,n-1} + V_D\right)^2 + {I_{L\_MAX}}^2} \tag{A.5}$$

$$\omega = \frac{1}{\sqrt{LC_{EG}}} \tag{A.6}$$

$$\theta = \sin^{-1}\left(\frac{-I_{L\_MAX}}{\sqrt{\frac{C_{EG}}{L}\left(V_{C,n-1} + V_D\right)^2 + {I_{L\_MAX}}^2}}\right) \tag{A.7}$$

Hence, the maximum inductor current, which is $I_{EQ,n}$, is

$$I_{EQ,n} = \sqrt{\frac{C_{EG}}{L}\left(V_{C,n-1} + V_D\right)^2 + {I_{L\_MAX}}^2} \tag{A.8}$$

By squaring and multiplying L/2 on both sides of (A.8), the equation yields the same result as (5.10), proofing that the energy balancing intuition is correct.

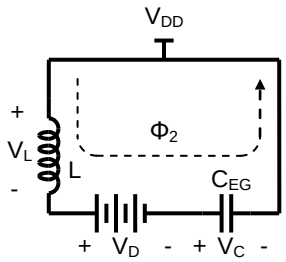


Figure A.1: Equivalent second-order circuit with negligible series resistance during the inductor de-energizing phase.

APPENDIX B

PCB FOR INTERFACING IC AND COMPUTER

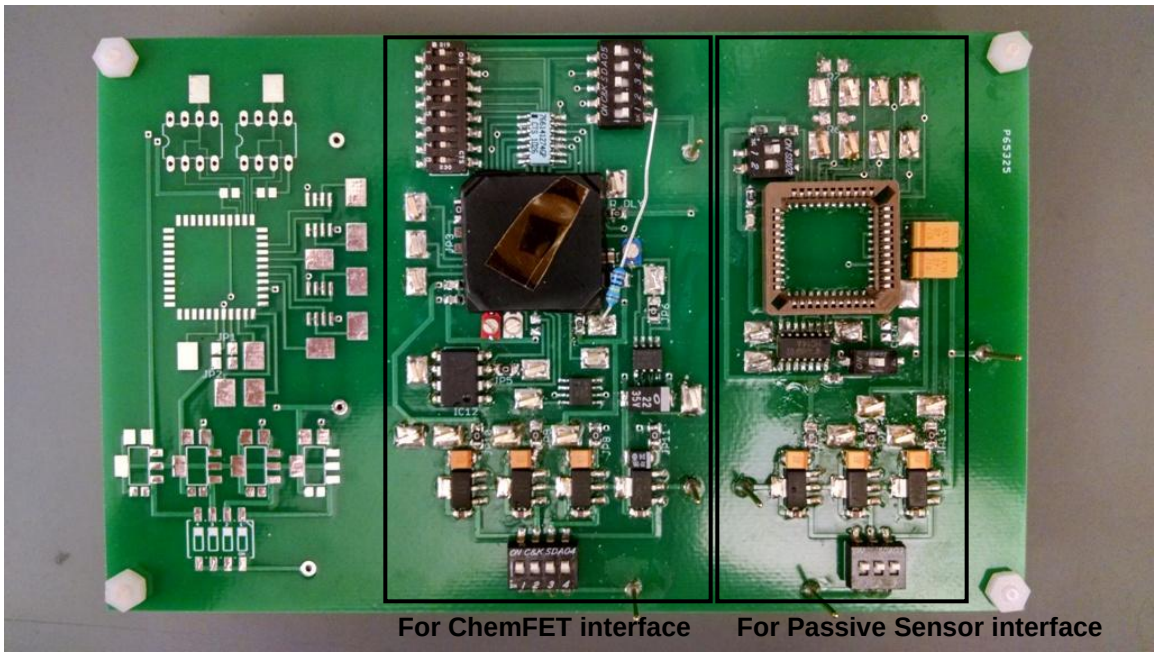


Figure B.1: Custom-made PCB including off-chip electronic components for powering and setting up the passive sensor and the ChemFET interfaces and providing communication between interfaces and computer.

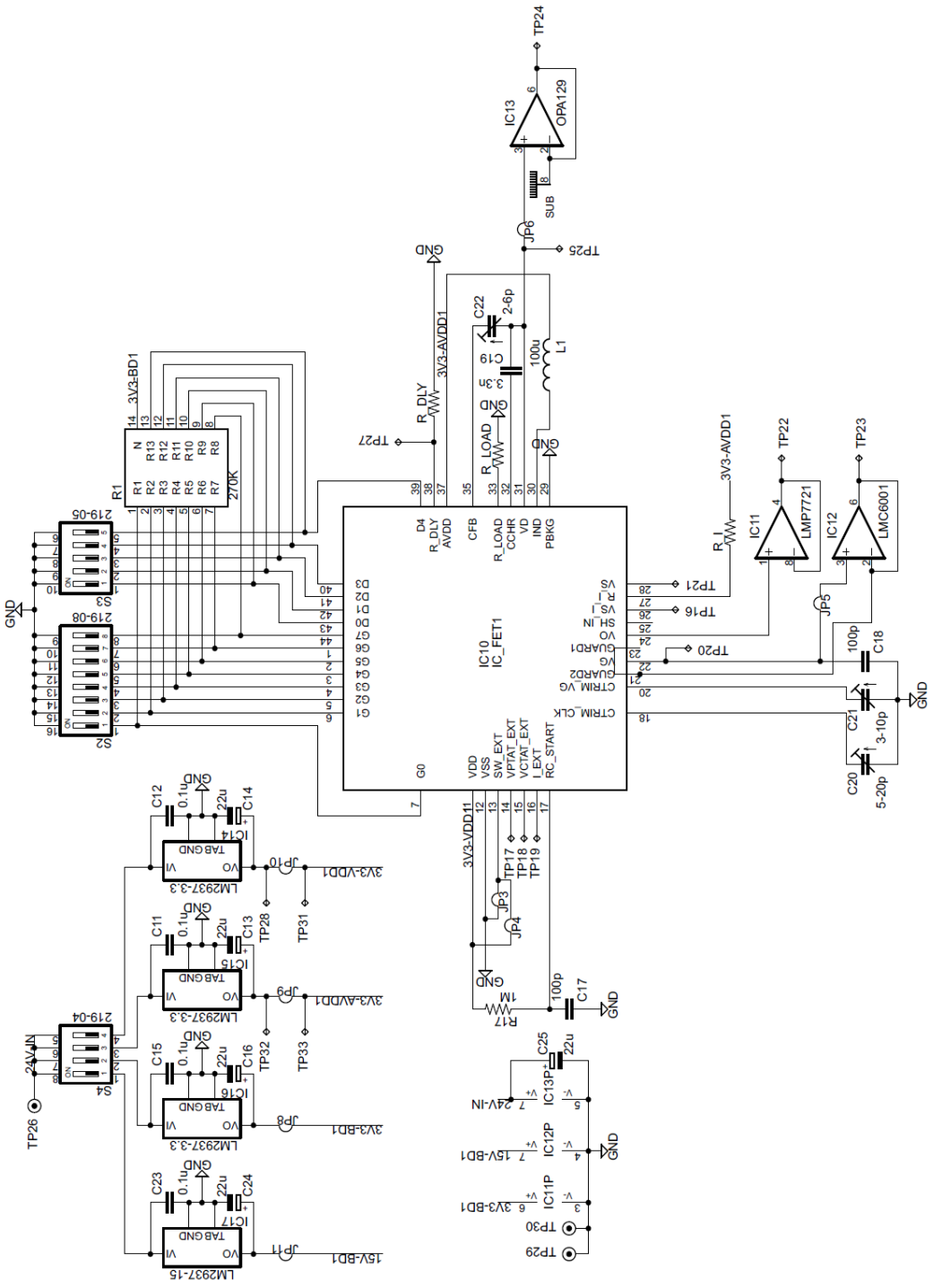


Figure B.2: Schematic of peripheral PCB circuits for the ChemFET interface.

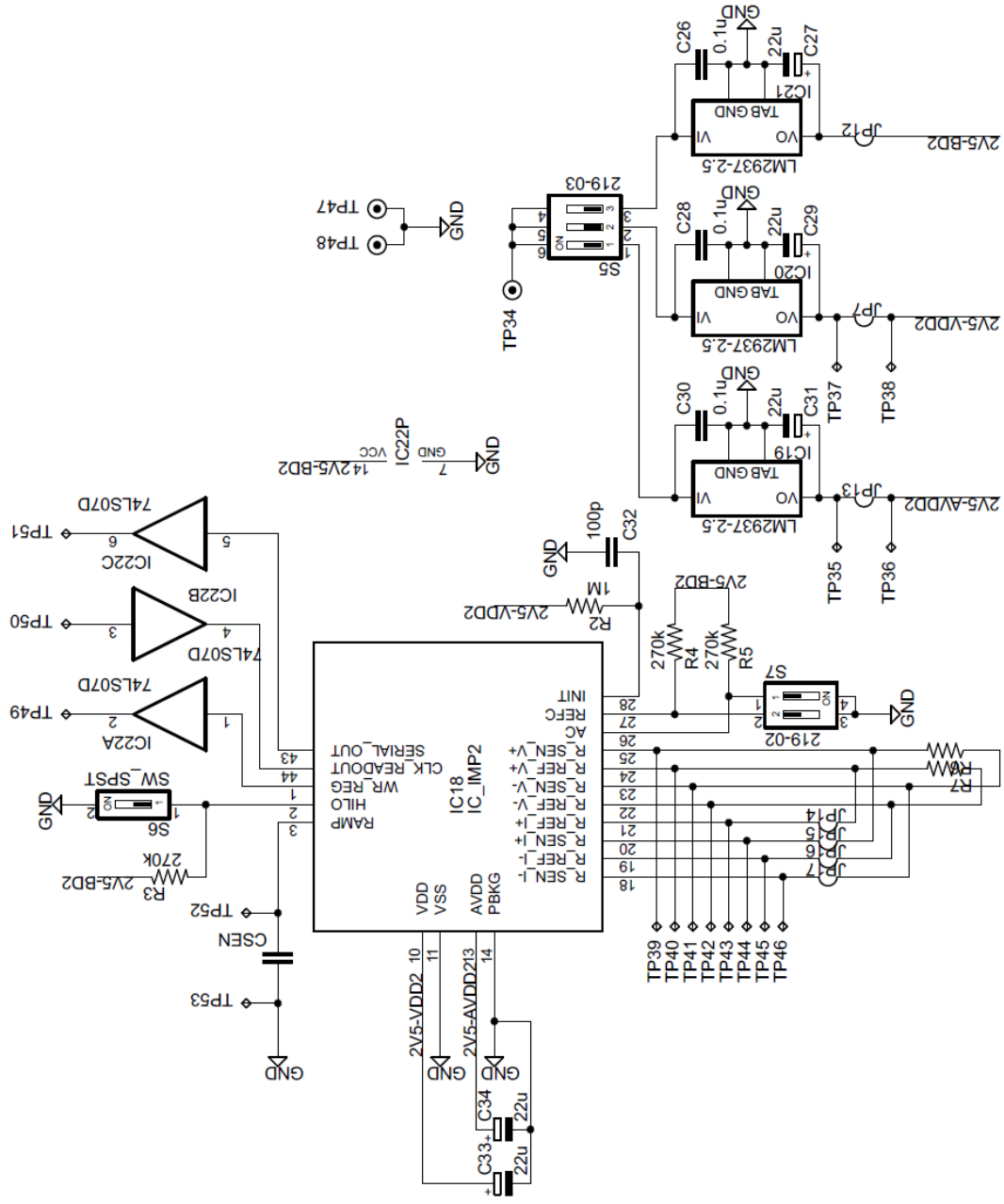


Figure B.3: Schematic of peripheral PCB circuits for the passive sensor interface.

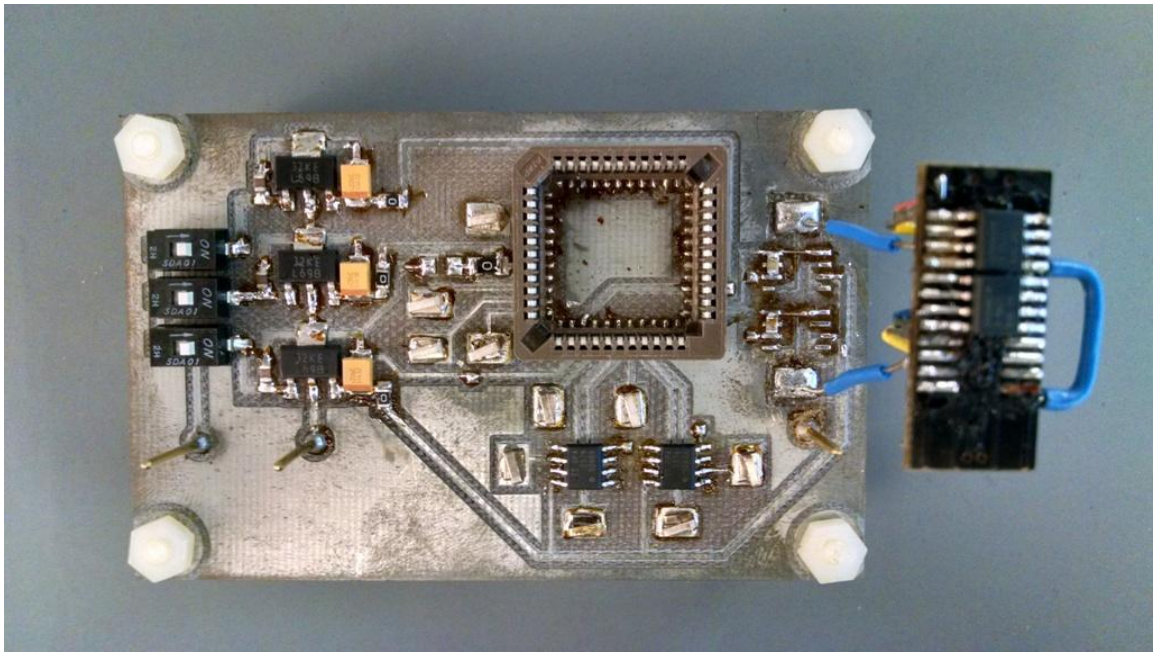


Figure B.4: Custom-made PCB including off-chip electronic components for testing three demonstrated BG-switch applications.

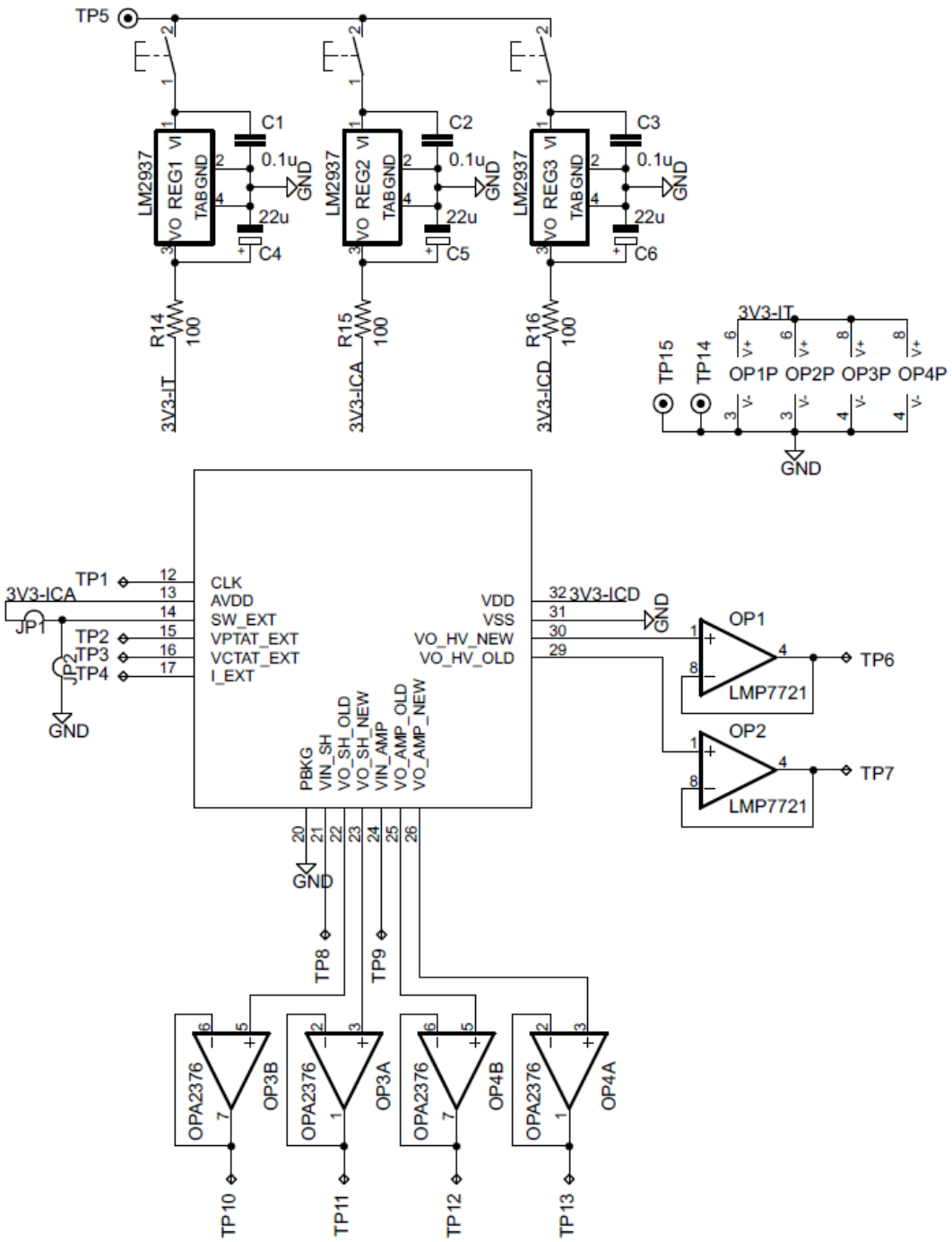


Figure B.5: Schematic of peripheral PCB circuits for the BG-switch testing die.

REFERENCES

[1] L. Zhang, F. Tian, and G. Pei, "A novel sensor selection using pattern recognition in electronic nose," *Measurement Journal of the International Measurement Confederation*, vol. 54, pp. 31-39, 2014.

[2] A. Amini, M. A. Bagheri, and G. A. Montzaer, "Improving gas identification accuracy of a temperature-modulated gas sensor using an ensemble of classifiers," *Sensor and Actuators B (Chemical)*, vol. 187, pp. 241-246, 2013.

[3] "7000C triple quadrupole GC/MS system," Agilent Technologies, Santa Clara, CA, USA (www.agilent.com).

[4] "EAGLE 2," RKI Instruments Inc., Union City, CA, USA (www.rkiinstruments.com).

[5] "GX-2009," RKI Instruments Inc., Union City, CA, USA (www.rkiinstruments.com).

[6] W. R. Collin, G. Serrano, L. K. Wright, H. Chang, N. Nunovero, and E. T. Zellers, "Microfabricated gas chromatograph for rapid, trace-level determinations of gas-phase explosive marker compounds," *Analytical Chemistry*, vol. 86, no. 1, pp. 655-663, 2014.

[7] "nest Smoke + CO Alarm," Nest Labs, Palo Alto, CA, USA (www.nest.com).

[8] C. Hagleitner, A. Hierlemann, D. Lange, A. Kummer, N. Kerness, O. Brand, and H. Baltes, "Smart single-chip gas sensor microsystem," *Nature*, vol. 414, no. 6861, pp. 293-296, 2001.

[9] J. Janata, M. Josowicz, P. Vanysek, D. M. DeVaney, "Chemical sensors," *Analytical Chemistry*, vol. 70, no. 12, pp. 179-208, 1998.

[10] B. Li, S. Santhanam, L. Schultz, M. Jeffries-EL, M. C. Iovu, G. Sauve, J. Cooper, R. Zhang, J. C. Revelli, A. G. Kusne, J. l. Snyder, T. Kowalewski, L. E. Weiss, R. D. McCullough, G .K. Fedder, and D .N. Lambeth, "Inkjet printed chemical sensor array based on polythiophene conductive polymers," *Sensors and Actuators B (Chemical)*, vol. 123, no. 2, pp. 651-660, 2007.

[11] D. L. McCorkle, R. J. Warmack, S. V. Patel, T. Mlsna, S. R. Hunter, and T. L. Ferrell, "Ethanol vapor detection in aqueous environments using micro-capacitors and dielectric polymers," *Sensor and Actuators B (Chemical)*, vol. 107, no. 2, pp. 892-903, 2005.

[12] W. P. Chan, B. Premanode, and C. Toumazou, "An integrated ISFETs instrumentation system in standard CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1924-1934, 2010.

[13] "SHT2x - Digital Humidity Sensor (RH/T)," Sensirion AG, Switzerland (www.sensirion.com/en/home/).

[14] N. Nizza, M. Dei, F. Butti, and P. Bruschi, "A low-power interface for capacitive sensors with PWM output and intrinsic low pass characteristic," *IEEE Transaction on Circuits and Systems I: Regular Papers*, vol. 60, no. 6, pp. 1419-1431, 2013.

[15] T. Siyama, A. Kato, K Fujiishi, and M. Nagatani, "A new detector for gaseous components using semiconducting thin films," *Analytical Chemistry*, vol. 34, no. 11, pp. 1502-1503, 1962.

[16] N. Taguchi, "A metal oxide gas sensor," Japanese Patent No. 45-38200, 1962.

[17] M. E. Franke, T. J. Koplin, and U. Simon, "Metal and metal oxide nanoparticles in chemiresistors: does the nanoscale matter?," *Small*, vol. 2, no. 1, pp. 36-50, 2006.

[18] "Figaro TGS2620 - for the detection of solvent vapors," Figaro Engineering Inc., Osaka, Japan (http://www.figarosensor.com/products/2620pdf.pdf).

[19] H. Lai and C. Chen, "Highly sensitive room-temperature CO gas sensors: Pt and Pd nanoparticle-decorated In_2O_3 flower-like nanobundles," *Journal of Materials Chemistry*, vol. 22, no. 26, pp. 13204-13208, 2012.

[20] U. Lange, N. V. Roznyatovskaya, and V. M. Mirsky, "Conducting polymers in chemical sensors and arrays," *Analytica Chemica Acta*, vol. 614, no. 1, pp. 1-26, 2008.

[21] S. Virji, J. Huang, R. B. Kaner, and B. H. Weiller, "Polyaniline nanofiber gas sensors: examination of response mechanisms," *Nano Letters*, vol. 4, no. 3, pp. 491-496, 2004.

[22] K. Sugiyasu and T. M. Swager, "Conducting-polymer-based chemical sensors: Transduction mechanisms," *Bulletin of the Chemical Society of Japan*, vol. 80, no. 11, pp. 2074-2083, 2007.

[23] P. N. Bartlett and J. H. Wang, "Electroactivity, stability and application in an enzyme switch at pH 7 of poly(aniline)-poly(styrenesulfonate) composite films," *Journal of the Chemical Society, Faraday Transactions*, vol. 92, no. 20, pp. 4137-4143, 1996.

[24] M. Cole, N. Ulivieri, J. Garcia-Guzman, and J. W. Gardner, "Parametric model of a polymeric chemoresistor for use in smart sensor design and simulation," *Microelectronics Journal*, vol. 34, no. 9, pp. 865-875, 2003.

[25] E. Llobet, "Gas sensors using carbon nanomaterials: a review," *Sensors and Actuators B (Chemical)*, vol. 179, pp. 32-45, 2013.

[26] T. Zhang, S. Mubeen, E. Bekyarova, B. Yoo, R. C. Haddon, N. V. Myung, and M. A. Deshusses, "Poly(m-aminobenzene sulfonic acid) functionalized single-walled carbon nanotubes based gas sensor," *Nanotechnology*, vol. 18, no. 16, 165504, 2007.

[27] M. C. Lonergan, E. J. Severin, B. J. Doleman, S. A. Beaber, R. H. Grubbs, and N. S. Lewis, "Array-Based vapor sensing using chemically sensitive, carbon black-polymer resistors," *Chemistry of Materials*, vol. 8, no. 9, pp. 2298-2312, 1996.

[28] B. C. Munoz, G. Steinthal, and S. Sunshine, "Conductive polymer-carbon black composites-based sensor arrays for use in an electronic nose," *Sensor Review*, vol. 19, no. 4, pp. 300-305, 1999.

[29] X.-J. Huang and Y.-K. Choi, "Chemical sensors based on nanostructured materials," *Sensors and Actuators B (Chemical)*, vol. 122, no. 1, pp. 659-671, 2007.

[30] S. Peng and K. Cho, "Chemical control of nanotube electronics," *Nanotechnology*, vol. 11, no. 2, pp. 57-60, 2000.

[31] T. Ishihara and S. Matsubara, "Capacitive type gas sensors," *Journal of Electroceramics*, vol. 2, no. 4, pp. 215-228, 1998.

[32] A. Botsialas, P. Oikonomou, D. Goustouridis, Th. Ganetsos, I. Raptis, and M. Sanopoulou, "A miniaturized chemocapacitor system for the detection of volatile organic compounds," *Sensors and Actuators B (Chemical)*, vol. 177, pp. 776-784, 2013.

[33] X. Li, S. Chen, and C. Feng, "Characterization of silicon nanoporous pillar array as room-temperature capacitive ethanol gas sensor," *Sensors and Actuators B (Chemical)*, vol. 123, no. 1, pp. 461-465, 2007.

[34] E. S. Snow, F. K. Perkins, E. J. Houser, S. C. Badescu, and T. L. Reinecke, "Chemical detection with a single-walled carbon nanotube capacitor," *Science*, vol. 307, no. 5717, pp. 1942-1945, 2005.

[35] A. Barbaro, C. Colapicchioni, E. Davini, G. Mazzamurro, A. P. Piotto, and F. Porcelli, "CHEMFET devices for biomedical and environmental applications," *Advanced Materials*, vol. 4, no. 6, pp. 402-408, 1992.

[36] Z. Gergintschew, P. Kornetzky, and D. Schipanski, "The capacitively controlled field effect transistor (CCFET) as a new low power gas sensor," *Sensors and Actuators B (Chemical)*, vol. B36, no. 1-3, pp. 285-289, 1996.

[37] P. Bergveld, "ISFET, Theory and Practice," *IEEE Sensor Conference*, in Toronto, Canada, 2003.

[38] L. Wang, D. Fine, D. Sharma, L. Torsi, and A. Dodabalapur, "Nanoscale organic and polymeric field-effect transistors as chemical sensors," *Analytical and Bioanalytical Chemistry*, vol. 384, no. 2, pp. 310-321, 2006.

[39] J. T. Mabeck and G. G. Malliaras, "Chemical and biological sensors based on organic thin-film transistors," *Analytical and Bioanalytical Chemistry*, vol. 384, no. 2, pp. 343-353, 2006.

[40] J.-M. Lee, I.-T. Cho, J.-H. Lee, and H.-I. Kwon, "Bias-stress-induced stretched-exponential time dependence of threshold voltage shift in IGZO thin film transistors," *Applied Physics Letters*, vol. 93, no. 9, pp. 093504, 2008.

[41] J. J. Siddiqui, J. D. Phillips, K. Leedy, and B. Bayraktaroglu, "Bias-temperature-stress characteristics of ZnO/HfO_2 thin-film transistors," *IEEE Transactions on Electron Devices*, vol. 59, no. 5, pp. 1488-1493, 2012.

[42] M. Andersson, R. Pearce, and A. L. Spetz, "New generation SiC based field effect transistor gas sensors," *Sensors and Actuators B (Chemical)*, vol. 179, pp. 96-106, 2013.

[43] F. V. Farmakis, Th. Speliotis, K. P. Alexandrou, C. Tsamis, M. Kompitsas, I. Fasaki, P. Jedrasik, G. Petersson, and B. Nilsson, "Field-effect transistors with thin ZnO as active layer for gas sensor applications," *Microelectronic Engineering*, vol. 85, no. 5-6, pp. 1035-1038, 2008.

[44] M. Gardon and J. M. Guilemany, "A review on fabrication, sensing mechanisms and performance of metal oxide gas sensors," *Journal of Materials Science: Materials in Electronics*, vol. 24, no. 5, pp. 1410-1421, 2013.

[45] H. Bai and G. Shi, "Gas sensors based on conducting polymers," *Sensors*, vol. 7, no. 3, pp. 267-307, 2007.

[46] H. Haick, "Chemical sensors based on molecularly modified metallic nanoparticles," *Journal of Physics D: Applied Physics*, vol. 40, no. 23, pp. 7173-7186, 2007.

[47] J. Lee, "Gas sensors using hierarchical and hollow oxide nanostructures: Overview," *Sensors and Actuators B (Chemical)*, vol. 140, no. 1, pp. 319-336, 2009.

[48] X. Chen, C. K. Y. Wong, C. A. Yuan, and G. Zhang, "Nanowire-based gas sensors," *Sensors and Actuators B (Chemical)*, vol. 177, pp. 178-195, 2013.

[49] S. Basu and P. Bhattacharyya, "Recent developments on graphene and graphene oxide based solid state gas sensors," *Sensors and Actuators B (Chemical)*, vol. 173, pp. 1-21, 2012.

[50] P. Bondavalli, P. Legagneux, and D. Pribat, "Carbon nanotubes based transistors as gas sensors: State of the art and critical review," *Sensors and Actuators B (Chemical)*, vol. 140, no. 1, pp. 304-318, 2009.

[51] "CR2477 non-rechargeable lithium battery," Panasonic Corporation, Osaka, Japan (na.industrial.panasonic.com).

[52] M. Grassi, P. Malcovati, and A. Baschirotto, "A 160 dB equivalent dynamic range auto-scaling interface for resistive gas sensors arrays," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 3, pp. 518-527, 2007.

[53] C. Falconi, C. D. Natale, E. Martinelli, A. D'Amico, E. Zampetti, J. W. Gardner, and C. M. Van Vliet, "1/f noise and its unusual high-frequency deactivation at high biasing currents in carbon black polymers with residual $1/f^{\gamma}$ ($\gamma = 2.2$) noise and a preliminary estimation of the average trap energy," *Sensors and Actuators B (Chemical)*, vol. 174, pp. 577-585, 2012.

[54] J. W. Gardner, P. K. Guha, F. Udrea, and J. A. Covington, "CMOS interfacing for integrated gas sensors: A review," *IEEE Sensors Journal*, vol. 10, no. 12, pp. 1833-1848, 2010.

[55] S. Joo and R. B. Brown, "Chemical sensors with integrated electronics," *Chemical Review*, vol. 108, no. 2, pp. 638-651, 2008.

[56] H. V. Shurmer and J. W. Gardner, "Odour discrimination with an electronic nose," *Sensors and Actuators B (Chemical)*, vol. B8, no. 1, pp. 1-11, 1992.

[57] J. W. Gardner, M. Vidic, P. Ingleby, A. C. Pike, J. E. Brignell, P. Scivier, P. N. Bartlett, A. J. Duke, and J. M. Elliott, "Response of a poly(pyrrole) resistive micro-bridge to ethanol vapour," *Sensors and Actuators B (Chemical)*, vol. B48, no. 1, pp. 289-295, 1998.

[58] N. Kordas, Y. Manoli, W. Mokwa, and M. Rospert, "A CMOS-compatible monolithic conductivity sensor with integrated electrodes," *Sensors and Actuators A (Physical)*, vol. A43, no. 1-3, pp.31-37, 1994.

[59] G. C. Cardinali, L. Dori, M. Fiorini, I. Sayago, G. Faglia, C. Perego, G. Sberveglieri, V. Liberali, F. Maloberti, and D. Tonietto, "A smart sensor system for carbon monoxide detection," *Analog Integrated Circuits and Signal Processing*, vol. 14, no. 3, pp. 275-296, 1997.

[60] B. Guo, A. Bermak, P. C. H. Chan, and G. -Z, Yan, "A monolithic integrated 4×4 tin oxide gas sensor array with on-chip multiplexing and differential readout circuits," *Solid-State Electronics*, vol. 51, no. 1, pp. 47-54, 2007.

[61] D. Barrettino, M. Graf, S. Taschini, S. Hafizovic, C. Hagleitner, and A. Hierlemann, "CMOS monolithic metal-oxide gas sensor microsystems," *IEEE Sensors Journal*, vol. 6, no. 2, pp. 276-286, 2006.

[62] K. T. Ng, F. Boussaid, and A. Bermak, "A CMOS single-chip gas recognition circuit for metal oxide gas sensor arrays," *IEEE Transactions on Circuits and System I: Regular Papers*, vol. 59, no. 7, pp. 1569-1580, 2011.

[63] T. S. Cho, K.-J. Lee, J. Kong, and A. P. Chandrakasan, " A 32-μ W 1.83-kS/s carbon nanotube chemical sensor system," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 659-669, 2009.

[64] X. Mu, E. Covington, D. Rairigh, C. Kurdak, E. Zellers, and A. J. Mason, "CMOS monolithic nanoparticle-coated chemiresistor array for micro-scale gas chromatography," *IEEE Sensors Journal*, vol. 12, no. 7, pp. 2444-2452, 2012.

[65] J. Garcia-Guzman, N. Ulivieri, M. Cole, and J. W. Gardner, "Design and simulation of a smart ratiometric ASIC chip for VOC monitoring," *Sensors and Actuators B (Chemical)*, vol. B95, no. 1-3, pp. 232-243, 2003.

[66] A. D'Amico, A. De Marcellis, C. Di Carlo, C. Di Natale, G. Ferri, E. Martinelli, R. Paolesse, and V. Stornelli, "Low-voltage low-power integrated analog lock-in amplifier for gas sensor applications," *Sensors and Actuators B (Chemical)*, vol. 144, no. 2, pp. 400-406, 2010.

[67] J. L. Merino, S. A. Bota, R. Casanova, A. Dieguez, C. Cane, and J. Samitier, "A reusable smart interface for gas sensor resistance measurement," *IEEE Transactions on Instrumentation and Measurement*, vol. 53, no. 4, pp. 1173-1178, 2004.

[68] M. Grassi, P. Malcovati, and A. Baschirotto, "A 141-dB dynamic range CMOS gas-sensor interface circuit without calibration with 16-bit digital output word," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 7, pp.1543-1554, 2007.

[69] S. Bagga, N. Bhat, and S. Mohan, "LPG gas-sensing system with SnO_2 thin-film transducer and 0.7-μm CMOS signal conditioning ASIC," *IEEE Transactions on Instrumentation and Measurement*, vol. 58, no. 10, pp. 3653-3658, 2009.

[70] G. Ferri, A. De Marcellis, C. Di Carlo, V. Stornelli, A. Flammini, A. Depari, D. Marioli, and E. Sisinni, "A CCII-based low-voltage low-power read-out circuit for DC-excited resistive gas sensors," *IEEE Sensors Journal*, vol. 9, no. 12, pp. 2035-2041, 2009.

[71] H. G. Dura, U. Schoneberg, B. J. Hostika, and H. Vogt, "Performance of hydrogen-sensitive MOS capacitances with integrated on-chip signal conditioning," *Sensors and Actuators B (Chemical)*, vol. B6, no. 1-3, pp. 162-164, 1992.

[72] Y. Y. Qiu, C. Azeredo-Leme, L. R. Alcacer, and J. E. Franca, "A CMOS humidity sensor with on-chip calibration," *Sensors and Actuators A (Physical)*, vol. A92, no.1-3, pp. 80-87, 2001.

[73] H. Baltes and E. Charbon, "Humidity-sensitive oscillator fabricated in double poly CMOS technology," *Sensors and Actuators B (Chemical)*, vol. B1, no. 1-6, pp. 441-445, 1990.

[74] M. Yang, C. Dai, P. Shih, and Y. Chen, "Cobalt oxide nanosheet humidity sensor integrated with circuit on chip," *Microelectronic Engineering*, vol. 88, no. 8, pp. 1742-1744, 2011.

[75] C. Cornila, A. Hierlemann, R. Lenggenhager, P. Malcovati, and H. Baltes, "Capacitive sensors in CMOS technology with polymer coating," *Sensors and Actuators B (Chemical)*, vol. B25, no. 1-3, pp. 357-361, 1995.

[76] T. Boltshauser, C. A. Leme, and H. Baltes, "High sensitivity CMOS humidity sensors with on-chip absolute capacitance measurement system," *Sensors and Actuators B (Chemical)*, vol. B15, no. 1-3, pp. 75-80, 1993.

[77] G. Ferri, C. Di Carlo, V. Stornelli, A. De Marcellis, A. Flammini, A. Depari, and N. Jand, "A single-chip integrated interfacing circuit for wide-range resistive gas sensor arrays," *Sensors and Actuators B (Chemical)*, vol. 143, no. 1, pp. 218-225, 2009.

[78] A. De Marcellis, A. Depari, G. Ferri, A. Flammini, and E. Sisinni, "A CMOS integrated low-voltage low-power time-controlled interface for chemical resistive sensors," *Sensors and Actuators B (Chemical)*, vol. 179, pp. 313-318, 2013.

[79] A. Manickam, A. Chevalier, M. McDermott, A. D. Ellington, and A. Hassibi, "A CMOS electrochemical impedance spectroscopy (EIS) biosensor array," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 6, pp. 379-390, 2010.

[80] C. Yang, S. R. Jadhav, R. M. Worden, and A. J. Mason, "Compact low-power impedance-to-digital converter for sensor array microsystems," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 10, pp. 2844-2855, 2009.

[81] P. Murali, K. Ranjit, N. Bhat, G. Banerjee, B. Amrutur, K. N. Bhat, and P. C. Ramamurthy, "A CMOS gas sensor array platform with fourier transform based impedance spectroscopy," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 11, pp. 2507-2517, 2012.

[82] K. Tsukada, T. Maruizumi, and H. Miyagi, "A multiple-ISFET integrated with CMOS interface circuits," *Electronics and Communications in Japan, Part 2 (Electronics)*, vol. 71, no. 12, pp. 93-99, 1988.

[83] B. Palan, F. V. Santos, J. M. Karam, B. Courtois, and M. Husak, "New ISFET sensor interface circuit for biomedical applications," *Sensors and Actuators B (Chemical)*, vol. B57, no. 1-3, pp. 63-68, 1999.

[84] L. Ravezzi and P. Conci, "ISFET sensor coupled with CMOS read-out circuit microsystem," *Electronics Letters*, vol. 34, no. 23, pp. 2234-2235, 1998.

[85] A. Thanachayanonot and S. Sirimasakul, "Ultra-low-power differential ISFET/REFET readout circuit," *ETRI Journal*, vol. 31, no. 2, pp. 243-245, 2009.

[86] W.-Y. Chung, Y.-T. Lin, D. G. Pijanowska, C.-H. Yang, M.-C. Wand, A. Krzyskow, and W. Torbicz, "New ISFET interface circuit design with temperature compensation," *Microelectronics Journal*, vol. 37, no. 10, pp. 1105-1114, 2006.

[87] W.-Y. Chung, C.-H. Yang, Y.-F. Wand, Y.-J. Chan, W. Torbicz, and D. G. Pijanowska, "A signal processing ASIC for ISFET-based chemical sensors," *Microelectronics Journal*, vol. 35, no. 8, pp. 667-675, 2004.

[88] P. K. Chan and D. Y. Chen, "A CMOS ISFET interface circuit with dynamic current temperature compensation technique," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 1, pp. 119-129, 2007.

[89] W. P. Chan, B. Premanode, and C. Toumazou, "An integrated ISFETs instrumentation system in standard CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1923-1934, 2010.

[90] P. A. Hammond, D. Ali, and D. R. S. Cumming, "A system-on-chip digital pH meter for use in a wireless diagnostic capsule," *IEEE Transactions on Biomedical Engineering*, vol. 52, no. 4, pp. 687-694, 2005.

[91] L. M. Shepherd and C. Toumazou, "A biochemical translinear principle with weak inversion ISFETs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 12, pp. 2614-2619, 2005.

[92] M. Kalofonou and C. Toumazou, "An ISFET based chemical Gilbert Cell," *Electronics Letters*, vol. 47, no. 16, pp. 903-904, 2011.

[93] J. Bausells, J. Carrabina, A. Errachid, and A. Merlos, "Ion-sensitive field-effect transistors fabricated in a commercial CMOS technology," *Sensors and Actuators B (Chemical)*, vol. B57, no. 1-3, pp. 56-62, 1999.

[94] Y.-L. Chin, J.-C. Chou, T.-P. Sun, H.-K. Liao, W.-Y. Chung, and S.-K. Hsiung, "A novel SnO_2/Al discrete gate ISFET pH sensor with CMOS standard process," *Sensors and Actuators B (Chemical)*, vol. B75, no. 1-2, pp. 36-42, 2001.

[95] A. Morgenshtein, L. Sudakov-Boreysha, U. Dinnar, C. G. Jakobson, and Y. Nemirovsky, "Wheatstone-Bridge readout interface for ISFET/REFET applications," *Sensors and Actuators B (Chemical)*, vol. B98, no. 1, pp. 18-27, 2004.

[96] A. Morgenshtein, L. Sudakov-Boreysha, U. Dinnar, C. G. Jakobson, and Y. Nemirovsky, "CMOS readout circuitry for ISFET microsystems," *Sensors and Actuators B (Chemical)*, vol. B97, no. 1, pp. 122-131, 2004.

[97] V. P. Chodavarapu, A. H. Titus, and A. N. Cartwright, "Differential read-out architecture for CMOS ISFET microsystems," *Electronics Letters*, vol. 41, no. 12, pp. 698-699, 2005.

[98] H.-S. Wong and M. H. White, "A CMOS-integrated `ISFET-operational amplifier' chemical sensor employing differential sensing," *IEEE Transactions on Electron Devices*, vol. 36, no. 3, pp. 479-487, 1989.

[99] P. Neuzil, "ISFET integrated sensor technology," *Sensors and Actuators B (Chemical)*, vol. B24, no. 1-3, pp. 232-235, 1995.

[100] C. Z. D. Goh, P. Georgiou, T. G. Constandinou, T. Prodromakis, and C. Toumazou, "A CMOS-Based ISFET chemical imager with auto-calibration capability," *IEEE Sensors Journal*, vol. 11, no. 12, pp. 3253-3260, 2011.

[101] Y. Liu, A. Al-Ahdal, P. Georgiou, and C. Tomazou, "Minimal readout scheme for ISFET sensing arrays based on pulse width modulation," *Electronics Letters*, vol. 48, no. 10, pp. 548-549, 2012.

[102] A. Hierlemann and R. Gutierrez-Osuna, "Higher-order chemical sensing," *Chemical Reviews*, vol. 108, no. 2, pp. 563-613, 2008.

[103] R. Ionescu, "Combined Seebeck and resistive SnO_2 gas sensors, a new selective device," *Sensors and Actuators B (Chemical)*, vol. B48, no. 1-3, pp. 392-394, 1998.

[104] J. A. Covington, S. L. Tan, J. W. Gardner, A. Hamilton, T. Koickal, and T. Pearce, "Combined smart chemFET-resistive sensor array," *Proceedings of IEEE Sensors 2003 (IEEE Cat. No.03CH37498)*, vol. 2, pp. 1120-1123, 2003.

[105] M. A. Urbiztondo, A. Peralta, I. Pellejero, J. Sese, M. P. Pina, I. Dufour, and J. Santamaria, "Detection of organic vapours with Si cantilevers coated with inorganic (zeolites) or organic (polymer) layers," *Sensors and Actuators B (Chemical)*, vol. 171-172, pp. 822-831, 2012.

[106] S. Dutta, S. D. Lewis, and A. Dodabalapur, "Hybrid organic/inorganic ambipolar thin film transistor chemical sensor," *Applied Physics Letters*, vol. 98, no. 21, pp. 213504, 2011.

[107] J. A. Hagen, S. N. Kim, B. Bayraktaroglu, K. Leedy, J. L. Chavez, N. Kelley-Loughnane, R. R. Naik, and M. O. Stone, "Biofunctionalized zinc oxide field effect transistors for selective sensing of riboflavin with current modulation," *Sensors*, vol. 11, no. 7, pp. 6645-6655, 2011.

[108] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488-492, 2004.

[109] J.-M. Lee, I.-T. Cho, J.-H. Lee, and H.-I. Kwon, "Bias-stress-induced stretched-exponential time dependence of threshold voltage shift in IGZO thin film transistors," *Applied Physics Letters*, vol. 93, no. 9, pp. 093504, 2008.

[110] J. J. Siddiqui, J. D. Phillips, K. Leedy, and B. Bayraktaroglu, "Bias-temperature-stress characteristics of ZnO/HfO_2 thin-film transistors," *IEEE Transactions on Electron Devices*, vol. 59, no. 5, pp. 1488-1493, 2012.

[111] H.-W. Zan, C.-H. Li, C.-C. Yeh, M.-Z. Dai, H.-F. Meng, and C.-C. Tsai, "Room-temperature-operated sensitive hybrid gas sensor based on amorphous indium gallium zinc oxide thin-film transistors," *Applied Physics Letters*, vol. 98, no. 25, pp. 253503, 2011.

[112] S. Pavlidis, J.-J Su, L. A. Beardslee, O. Brand, J. A. Hagen, N. Kelley-Loughnane, and P. Leclaire, " Pulsed operation of IGZO TFTs for VOC sensing applicationss," *Proceedings of IEEE Sensors*, 2012.

[113] T. Sepke, P. Holloway, C. G. Sodini, and H.-S. Lee, "Noise Analysis for Comparator-Based Circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 3, pp. 541-553, 2009.

[114] M. S. Keshner, "1/f noise," *Proceedings of the IEEE*, vol. 70, no. 3, pp. 212-218, 1982.

[115] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design 2nd edition*. New York: Oxford University Press, Inc., 2002.

[116] F. Veirano, P. Perez, S. Besio, P. Castro, and F. Silveira, "Ultra low power pulse generator based on a ring oscillator with direct path current avoidance," *2013 IEEE 4th Latin American Symposium on Circuits and Systems (LASCAS)*, 2013.

[117] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 6, pp. 790-804, 1999.

[118] J. Yu, F. F. Dai, and R. C. Jaeger, "A 12-Bit Vernier ring time-to-digital converter in 0.13μm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 830-842, 2010.

[119] "34401A Digital Multimeter, 6 1/2 Digit," Agilent Technologies, Santa Clara, CA, USA (www.agilent.com).

[120] "4284A Precision LCR Meter, 20Nz to 1MHz," Agilent Technologies, Santa Clara, CA, USA (www.agilent.com).

[121] H.-J. Ryoo, S.-H. Ahn, J.-W. Gong, and S.-R. Jang, "Design and comparison of capacitor chargers for solid-state pulsed power modulator," *IEEE Transactions on Plasma Science*, vol. 41, no. 10, pp. 2675-2683, 2013.

[122] V. Brommer, O. Liebfried, and S. Scharnholz, "A high-power capacitor charger using IGCTs in a boost converter topology," *IEEE Transactions on Plasma Science*, vol. 41, no. 10, pp. 2600-2604, 2013.

[123] A. Pokryvailo, C. Carp, and C. Scapellati, "High-power high-performance low-cost capacitor charger concept and implementation," *IEEE Transactions on Plasma Science*, vol. 38, no. 10, pp. 2734-2745, 2010.

[124] A. Hren, J. Korelic, and M. Milanovic, "RC-RCD clamp circuit for ringing losses reduction in a flyback converter," *IEEE Transaction on Circuits and Systems II: Express Briefs*, vol. 53, no. 5, pp. 369-373, 2006.

[125] G. K. Balachandran and P. E. Allen, "Fully differential switched-current memory cell with low charge-injection errors," *IEE Proceedings-Circuits, Devices and Systems*, vol. 148, no. 3, pp. 157–164, 2001.

[126] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proceedings of the IEEE*, vol. 91, no. 2, pp. 305–327, 2003.

[127] Y. Lin, A. Wu, C. Chang, R. Yang, W. Chen, J. Liaw, and C. H. Diaz, "Leakage scaling in deep submicron CMOS for SoC," *IEEE Transactions on Electron Devices*, vol. 49, no. 6, pp. 1034–1041, 2002.

[128] Y. Taur and E. J. Nowak, "CMOS devices below 0.1μm: how high will performance go?," in *IEDM Technical Digest*, 1997, pp. 215-218.

[129] S.-H. Lo, D. A. Buchanan, and Y. Taur, "Modeling and characterization of quantization, polysilicon depletion, and direct tunneling effects in MOSFETs with ultrathin oxides," *IBM Journal of Research and Development*, vol. 43, no. 3, pp. 327–337, 1999.

[130] K. F. Schuegraf and C. Hu, "Hole injection SiO_2 breakdown model for very low voltage lifetime extrapolation," *IEEE Transaction on Electron Devices*, vol. 41, no. 5, pp. 761–767, 1994.

[131] S. Yuan, Y. Li, Y. Yuan, and Y. Liu, "Pass transistor with dual threshold voltage domino logic design using standby switch for reduced subthreshold leakage current," *Microelectronics Journal*, vol. 44, no. 12, pp. 1099–1106, 2013.

[132] H. Kim, B. H. Lee, J. Kim, J. Y. Choi, K. Choi, and Y. Shin, "Supply switching with ground collapse for low-leakage register files in 65-nm CMOS," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 18, no. 3, pp. 505–509, 2010.

[133] A. Valentian and E. Beigne, "Automatic gate biasing of an SCCMOS power switch achieving maximum leakage reduction and lowering leakage current variability," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 7, pp. 1688–1698, 2008.

[134] H. Kawaguchi, K. Nose, and T. Sakurai, "A super cut-off CMOS (SCCMOS) scheme for 0.5-V supply voltage with picoampere stand-by current," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 10, pp. 1498–1501, 2000.

[135] K. Ishida, K. Kanda, A. Tamtrakarn, H. Kawaguchi, and T. Sakurai, "Managing subthreshold leakage in charge-based analog circuits with low-VTH transistors by analog T- switch (AT-switch) and super cut-off CMOS (SCCMOS)," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 4, pp. 859–867, 2006.

[136] L. Zou, J. Pathrose, K. T. C. Chai, M. Je, and Y. P. Xu, "Sample-and-hold circuit with dynamic switch leakage compensation," *Electronics Letters*, vol. 49, no. 21, pp. 1323–1325, 2013.

[137] L. S. Y. Wong, S. Hossain, A. Ta, J. Edvinsson, D. H. Rivas, and H. Naas, "A very low-power CMOS mixed- signal IC for implantable pacemaker applications," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2446–2456, 2004.

[138] Y. Peng, Y. M. Shkel, and G.-H. Kim, "Stress dielectric response in liquid polymers," *Journal of Rheology*, vol. 49, no. 1, pp. 297-311, 2005.